# Wafer characterization tests MAIA BEE project

Overview
Wafer characterization
Sensor test
In situ debug and maintenance DAQ

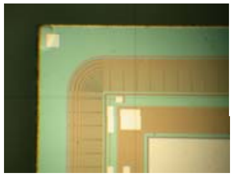
LPC LAL LLR

# Instrumental chain ongoing work at LPC
# from Wafer to data acquisition

ASU = Active Sensor Unit

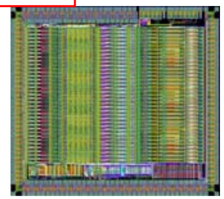
**Detector**

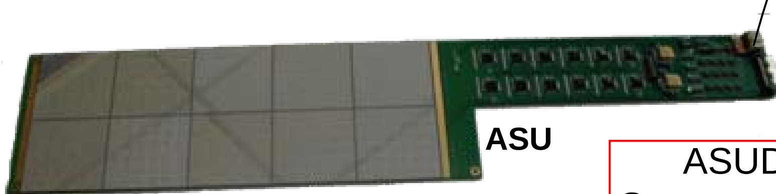
**Wafer**



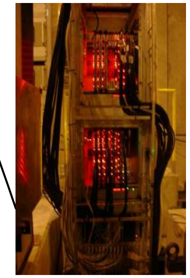
**VFE**

**SKiROC**



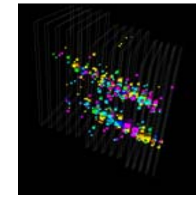



**Read-out DAQ**



**Test bench**

**Analysis Software**



Wafer
Crosstalk studies
Design validation

ASUDAQ
Sensor validation
Cosmic tests

ISDDAQ
Debug, Monitoring
Maintainance

SW reconstruction

## ASUDAQ prototype

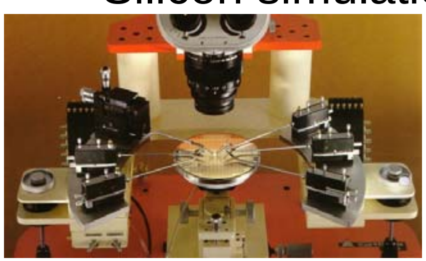
- first developments of a generic design

## Wafer test bench being set up

- 3x3 Test wafers specifications
- Probe tips test apparatus
- Silicon simulation tools

## ISDDAQ architecture issue

- On beam integration
- Architecture level R&D



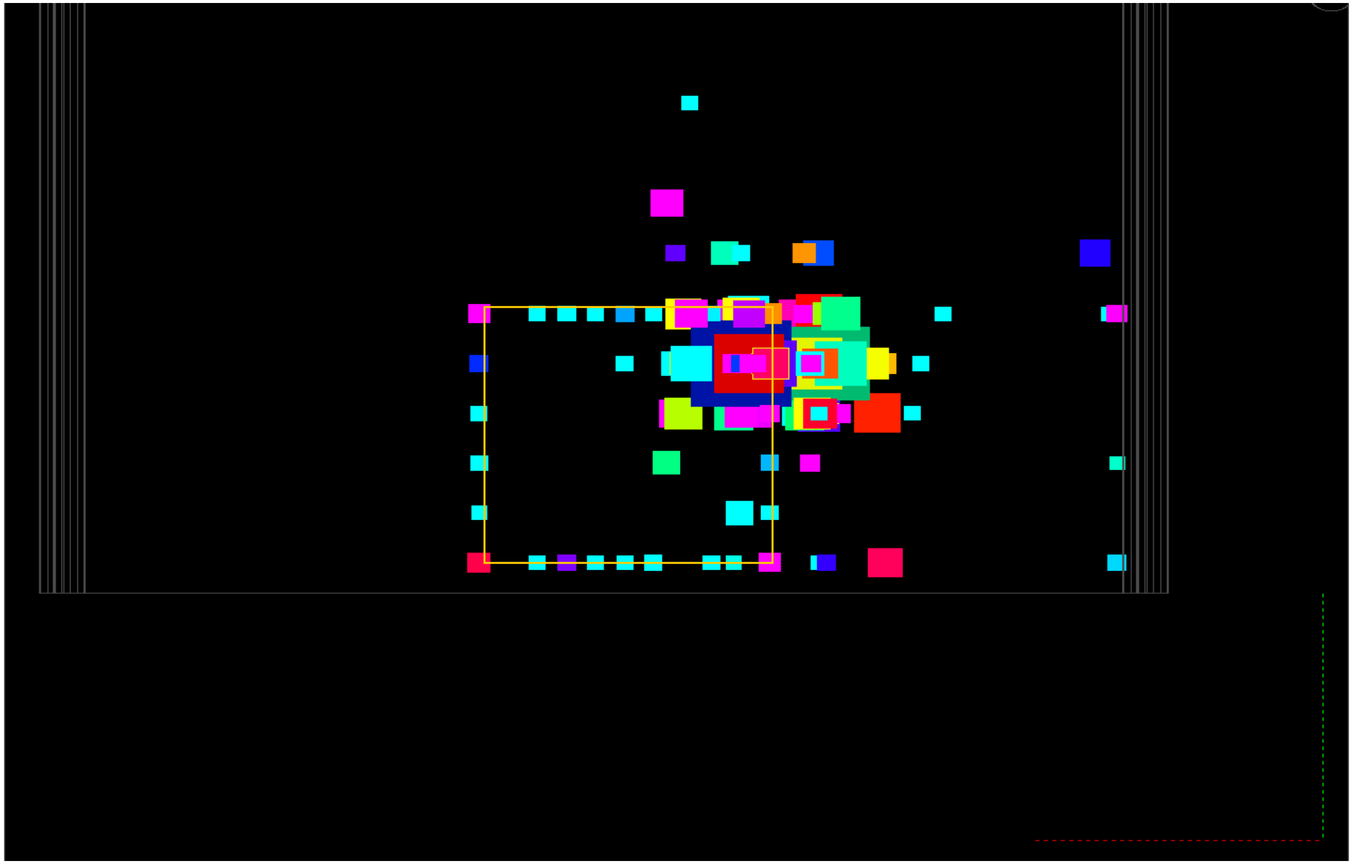
**Towards EUDET**,
Validation & Test of the whole chain

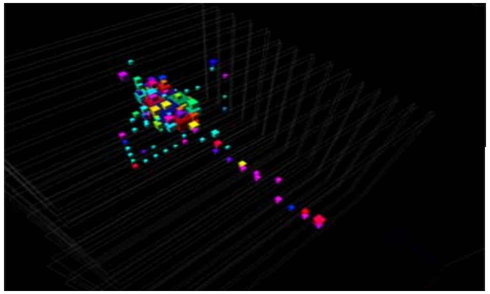
- R&D test tools for sensor and electronics
- Validation, debugging and maintenance on beam

Part I

# Wafer

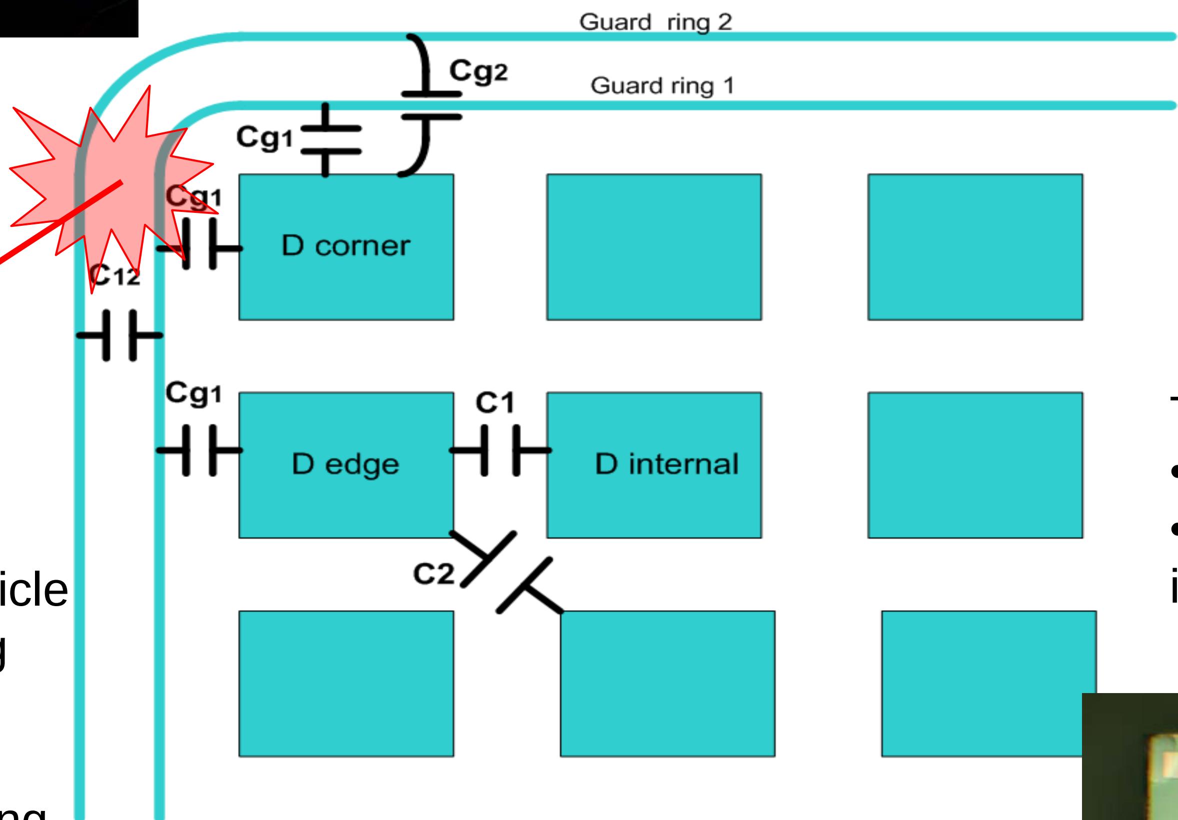
Unexpected behavior seen during test beam : SQUARE events !
Unmatched pattern according to physics models…
Has to be understood and solved





# Wafer

**Understand Square events origins**
**Crosstalk studies according to design options**

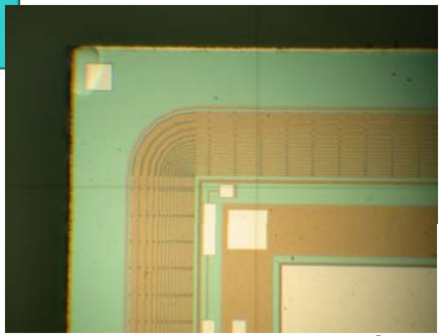



Effects of a particle hit on guard ring could be propagated to every bordering pixels

Try to reproduce the phemenon

Test new designs
• layout
• technologic improvements

**Various 3x3 test wafer to be produced by OnSemi**
**As result, select the best design technique…**



# Wafers : Method

**Square event**

**Understand**

**Simulation**

SILVACO

**Guardring design**

- Splited
- Polarized
- Progressive

Effects on
- Leakage
- Capacitance

**Charge injection**

- Photon
- Electron

Current flow

SPICE

**Pure crosstalk**

Electrical level

**Physical Model**

Splited guardring impact on pure crosstalk

**Characterize**

**Measurment Bench**

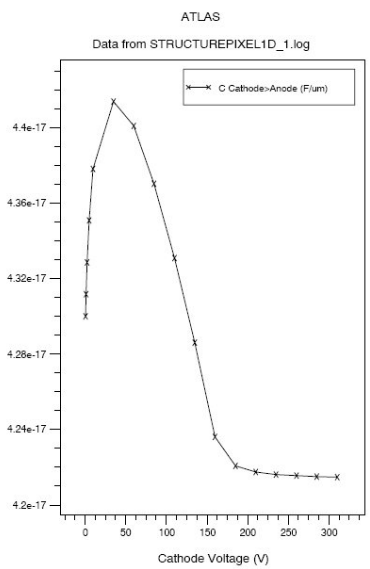
**Samples**

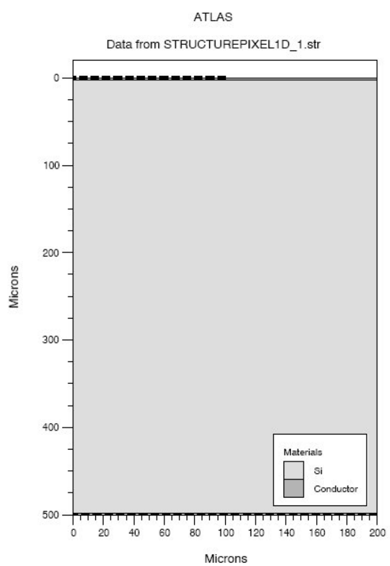
Find out best candidate

Cu-Epo "wafer"

3x3 pixels test wafers

# SILVACO SIMULATIONS




C(V) between pixel and common bias and C(V,f,a,b,c,d…)

First step to verify capacitance values between pixels, guardrings, substrate

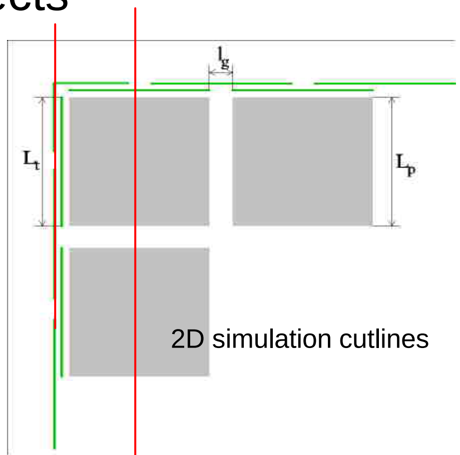
Then back annotate to SPICE simulation

Simulated Cap. Values are within a 20% range from expected values calculated with first order formula

3D simulation are ongoing to take into account border effects

Second step to simulate ionization effects (electron or photon) or SEE/SEU events

Third step (following months) to evaluate design parameters impact on C and explore new designs of guardrings from crosstalk point of view



## Segmented guardring technique may prevent Xtalk by a factor 3

**diaphonie pixel – 3x3 matrix**
Cgb = 4 pF Cgg=24pF Cpg = 1 pF

# SPICE

Calorimeter for ILC

### Plain guardring

| | | | | |
|---|---|---|---|---|
| 5.6 | | 5.6 | | 5.6 |
| | 1 | 100 | 1 | |
| 5.6 | 0.3 | | 0.3 | 5.6 |
| | 0.5 | 0.3 | 0.5 | |
| 5.6 | | 5.6 | | 5.6 |

### Segmented guardring

160 fF

| | | | | |
|---|---|---|---|---|
| 2 | | 42 | | 2 |
| | 0.3 | 100 | 0.3 | |
| 2 | 0.1 | - | 0.1 | 2 |
| | 0.15 | 0.08 | 0.15 | |
| 2 | | 2 | | 2 |

Guardring **non segmenté**, **Signal at G1**

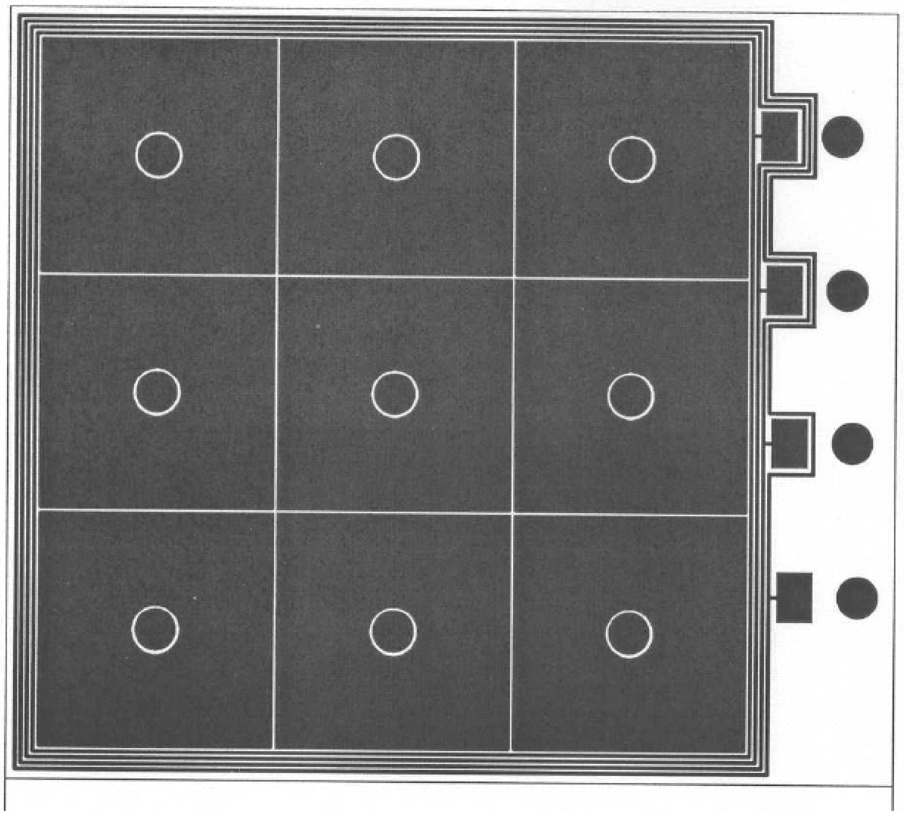
| | | | | |
|---|---|---|---|---|
| | | 100 | | |
| | 20 | 5.6 | 20 | |
| | 5.6 | - | 5.6 | |
| | 20 | 5.6 | 20 | |
| | | | | |

Guardring 1 segmenté, **Signal at G1_2 segment**, Css=160 fF

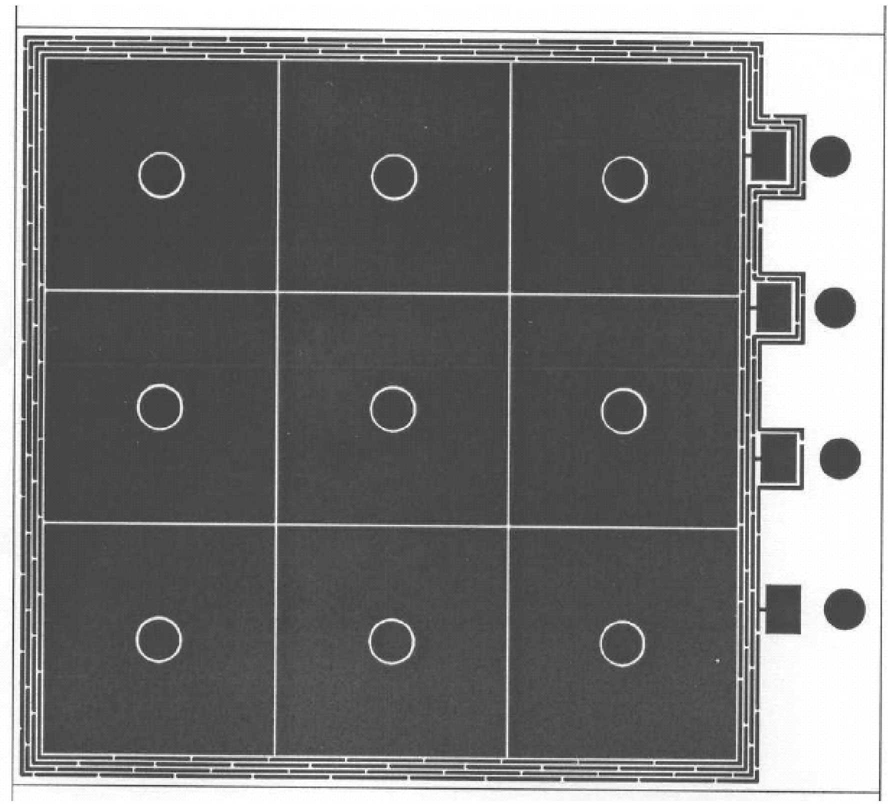
| | | | | |
|---|---|---|---|---|
| 6 | | 100 | | 6 |
| | 1 | 5.6 | 1 | |
| 4 | 0.2 | - | 0.2 | 4 |
| | 0.4 | 0.2 | 0.4 | |
| 4 | | 4 | | 4 |

# Physical Model : Cu-Epoxy

- Study pure crosstalk effects (various configurations)
- Measurement method validation
- Test bench calibration



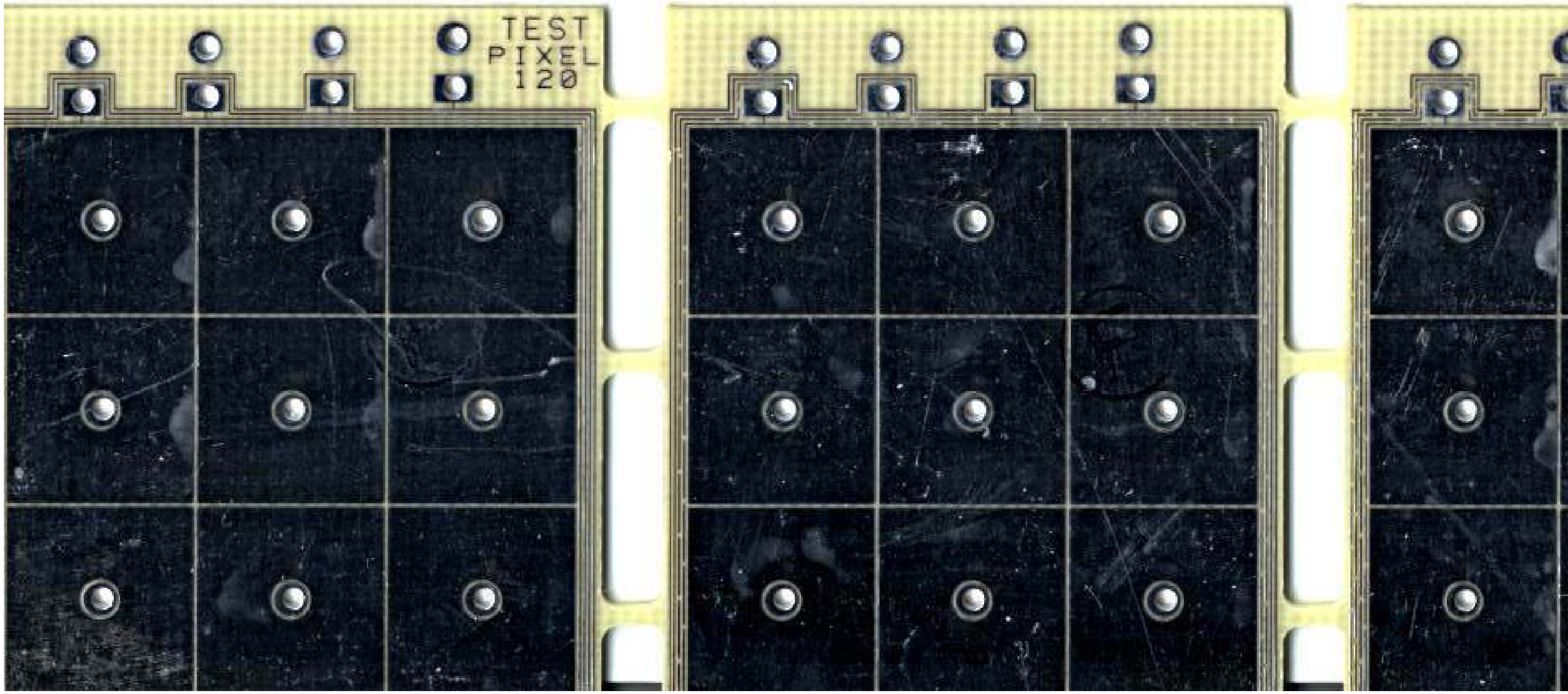
Continuous guardring

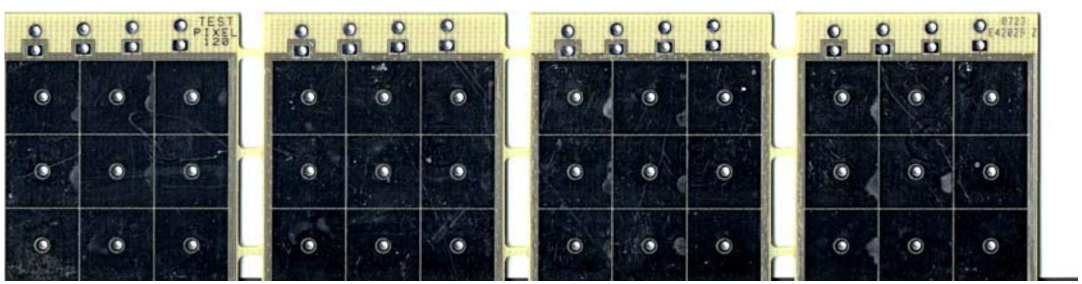


Splited guardring

- 4 @ 1 cm
- 4 @ 3 mm
- 2 @ 1 cm + 2 unsplited

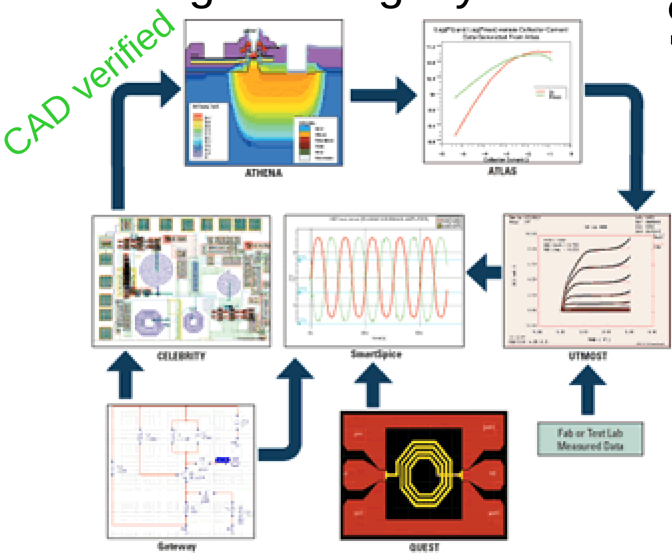
# Physical Model : Cu-Epoxy

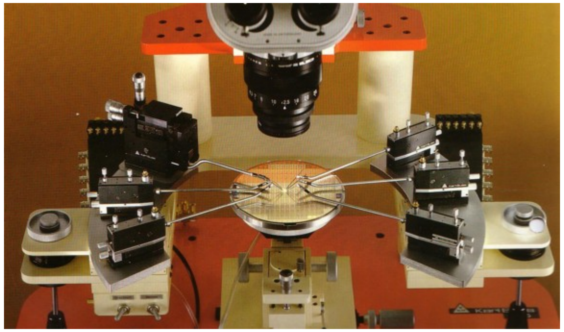


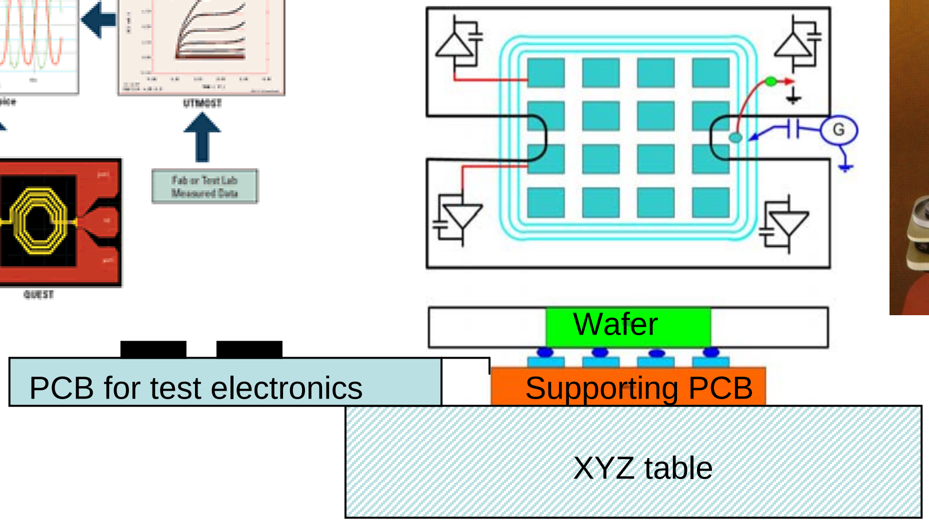



# Wafer
## Setup and tools

**Simulation**
- capacitive coupling
- guard ring layout

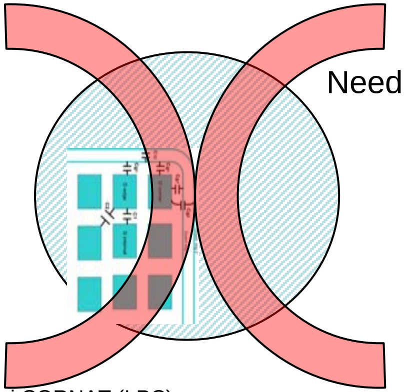





**Characterization**
- Charge injection
- pixel signal analysis

**Test bench**
- pulse generator
- micropositioner & probes
- shaper + scope

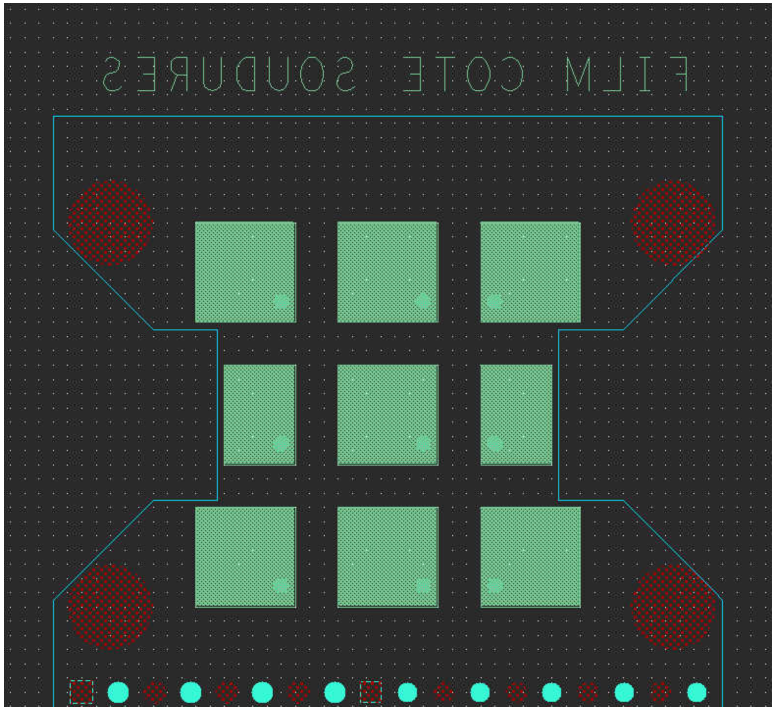


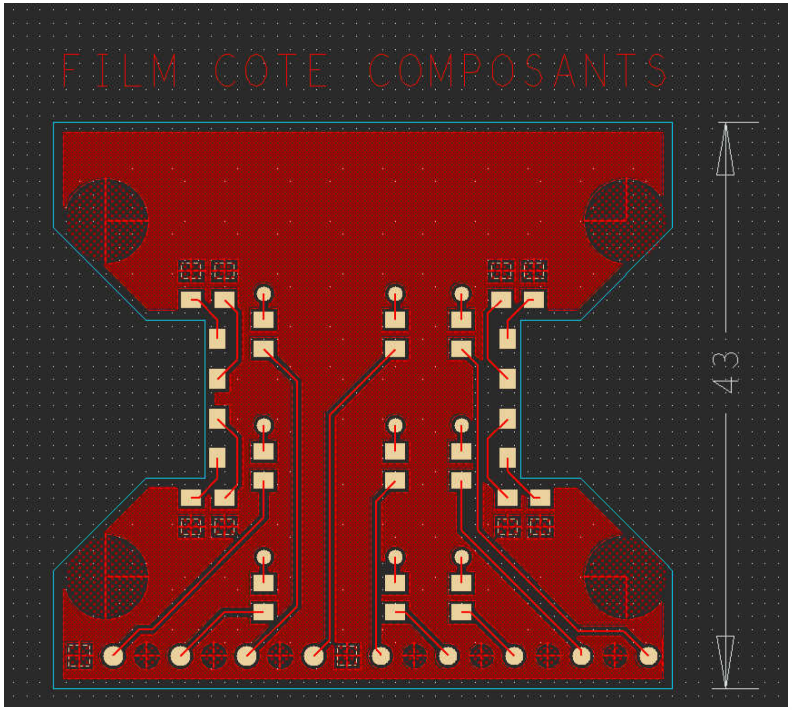

I(V) / C(V) ?

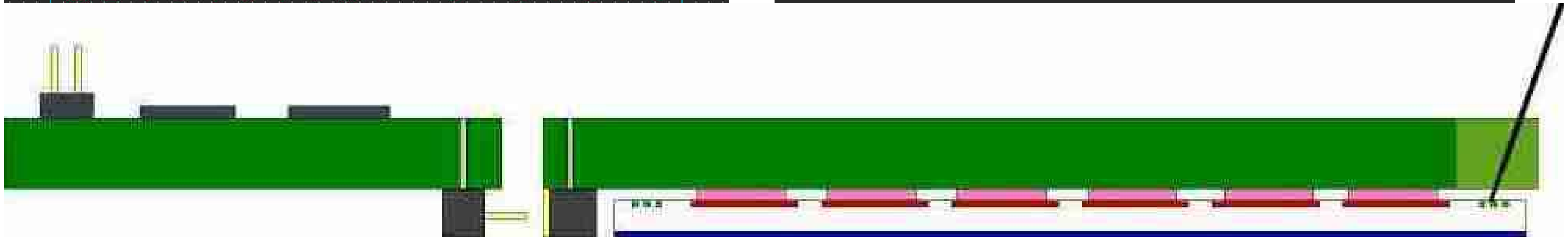
OPEN QUESTION

# PCB to glue 3x3 test wafers

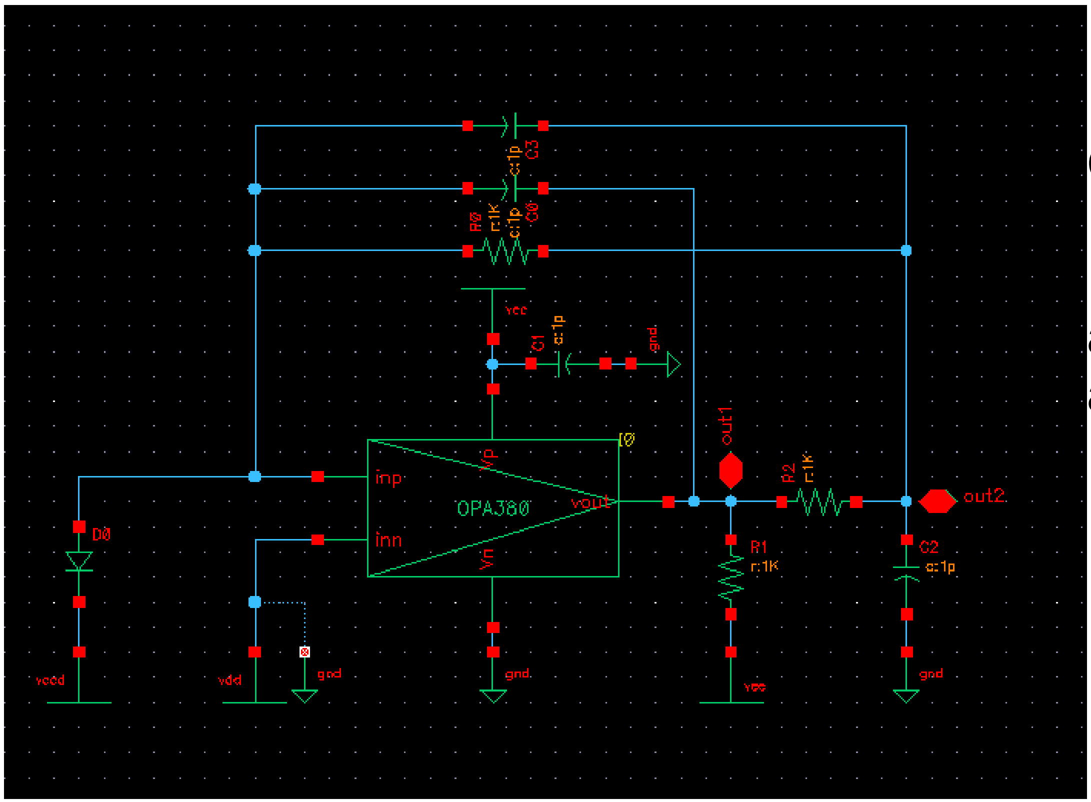
Sent to fab. Last week



# Instrumentation board




OPA380 or OPA657

Sent to fab. Last week

Compatible with wafer gluing PCB

Includes 3 OPA for signal shaping and transimpedance adaptation to a scope

Nice picture of the board here

# Wafer
## actions

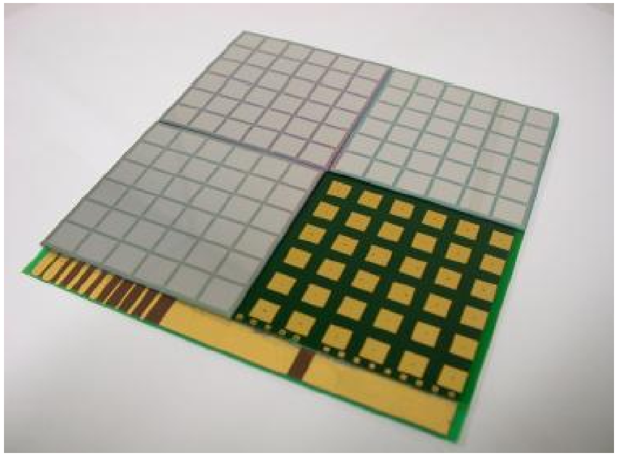
= done or good results

= on going

- Simulation
  - Software know-how & test case (first try on 10th of april)
  - **Simulate :** depletion area between segments, polarization effects, photon or electron effects, capacitance extraction, multiple pixels and guardring, 3D
  - **Comparison with test beam data** (may validate "pure crosstalk" hypothesis)

- Physical Model
  - Layout
  - Simulations (Spectraa, spice)
  - Bench tests during July
- Measurement bench
  - Assembly (black box, Keithley,…)
  - Test board design
    - Connector
    - Charge injector
    - **Shaper**
  - **3x3 matrix specifications**
    - **Back from fab. on oct/nov**
    - **Measurements will follow**
- Interaction with manufacturer
  - **Layout options**
  - **Common wafer floorplan**

Proposal J-C. V.



# MAIA BEE
(Y)

M aintenance
A pparatus
I ncluding (data)
A cquisition (on)

B eam (for)
E UDET
E CAL

{ASUDAQ, ISDDAQ} = MAIA BEE

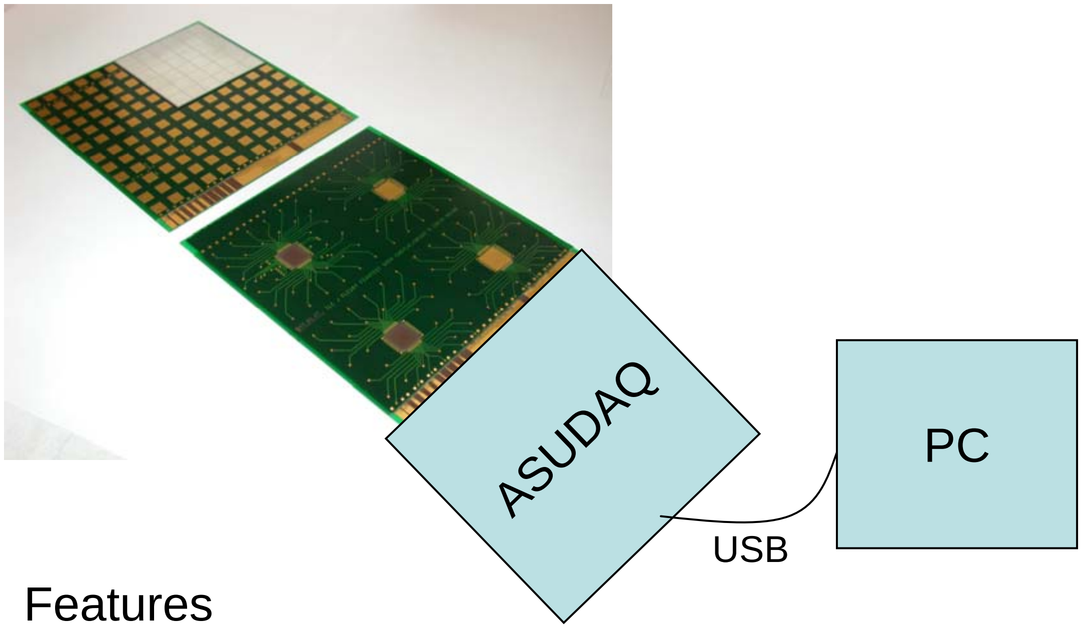
ASUDAQ = ASU DAQ

ASUDAQ = In Situ Debug DAQ (of one SLAB)

# ASUDAQ

## Cosmic test of ASU

**A**ctive **S**ensor **U**nit




**Cosmic test bench** for ASU characterization.

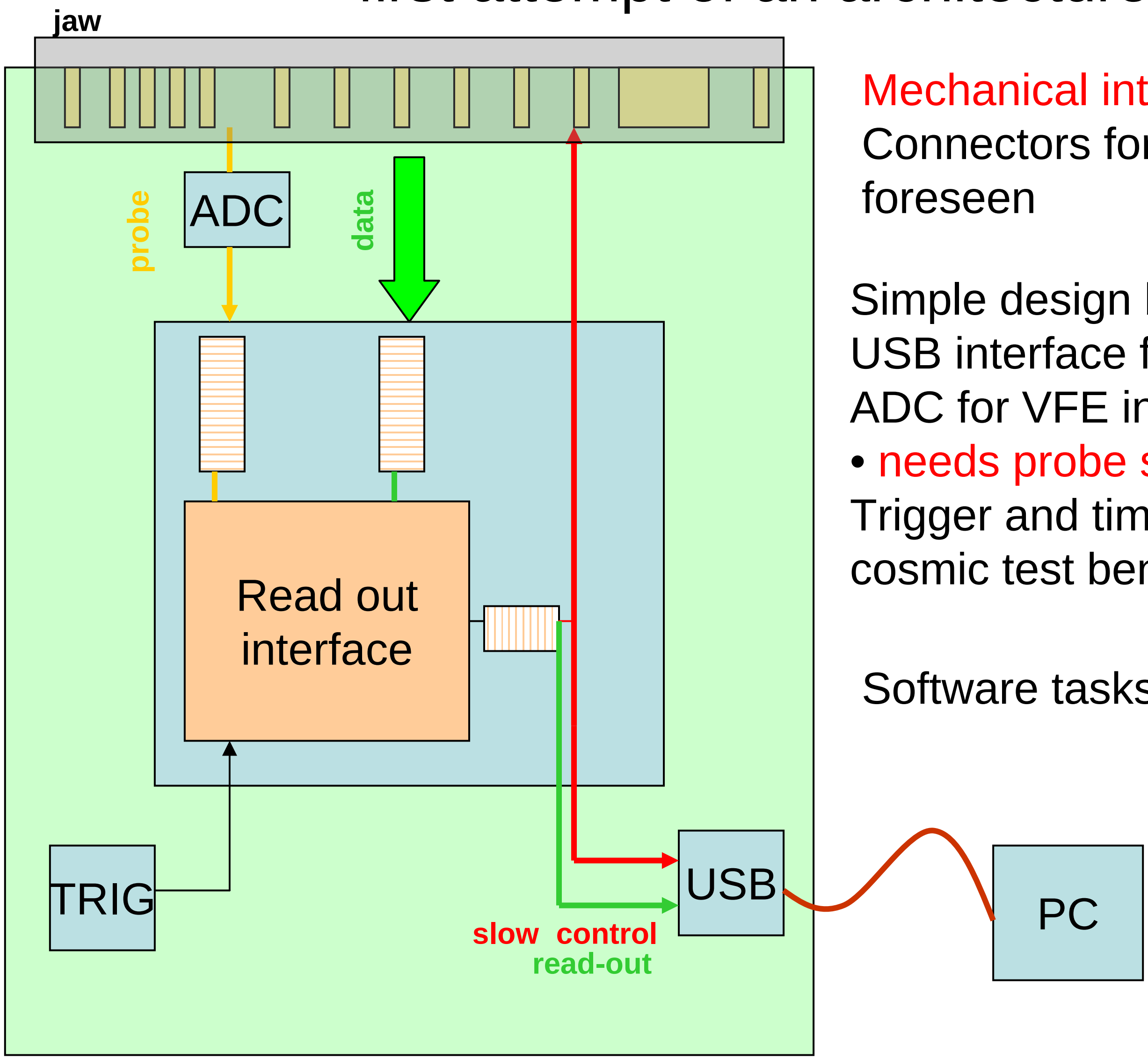
First R&D step towards EUDET production tests

Features
- full **slow control** including internal probing system control
- access to analog test points (embedded ADC)
- **read out** of 4 SKiROC through USB & PC
- cosmic bench environment support (triggers)
- mechanical jaw providing damageless contacts to ASU

A board is being designed : schematic mostly done

# ASUDAQ

## first attempt of an architecture




Mechanical interface ?

Connectors for 1-4 ASU can be foreseen

Simple design based on FPGA

USB interface for PC

ADC for VFE internal probing system

- needs probe signal on ASU connector

Trigger and timing signals for cosmic test bench

Software tasks to be specified

OPEN QUESTION

# ASUDAQ
## ASU connector

ASU/SLAB connector I/O LPC 22/06/07

| CAT | NAME | | | |
|---|---|---|---|---|
| HV | | | | |
| POWER | GND | 1 | | |
| | 3.3V | 1 | | |
| BIAS | | 0 | | |
| REFERENCE | | 0 | | |
| CCC | clkp 40MHz | 1 LVDS | O | |
| | clkn 40MHz | | | |
| | Reset | 1 OC | OC | |
| | power_on_xxxx | 5 LVTTL | O | new 22/06 |
| | testin | analogue | O | new 22/06 |
| SC | clk_sc | 1 LVTTL | O | |
| | rstb_sc | 1 LVTTL | O | |
| | sroutscbuf | 1 LVTTL | I | |
| | srin_sc | 1 LVTTL | O | |
| PROBE | analogue_probe | analogue | Ain | |
| | digital_probe | 1 LVTTL | I | |
| READOUT | clkp_5MHz / 1 MHz | 1 LVDS | O | |
| | clkn_5MHz / 1 MHz | | | |
| | StartAcq | 1 LVTTL | O | |
| | ValEvtp | 1 LVDS | O | |
| | ValEvtn | | | |
| | RazChnp | 1 LVDS | O | |
| | RazChnn | | | |
| | StartReadOut | 1 LVTTL | O | |
| | EndReadOut | 1 LVTTL | I | |
| | TransmitOn | 1 LVTTL | I | |
| | Dout (out0) | 1 LVTTL | I | |
| | RamFull | 1 OC | OC | |
| | TriggerExt | 1 LVTTL | O | |
| | TriggerOut | 1 LVTTL | I | |

To be discussed

More I/O added
to current board to follow
SKiROC developments

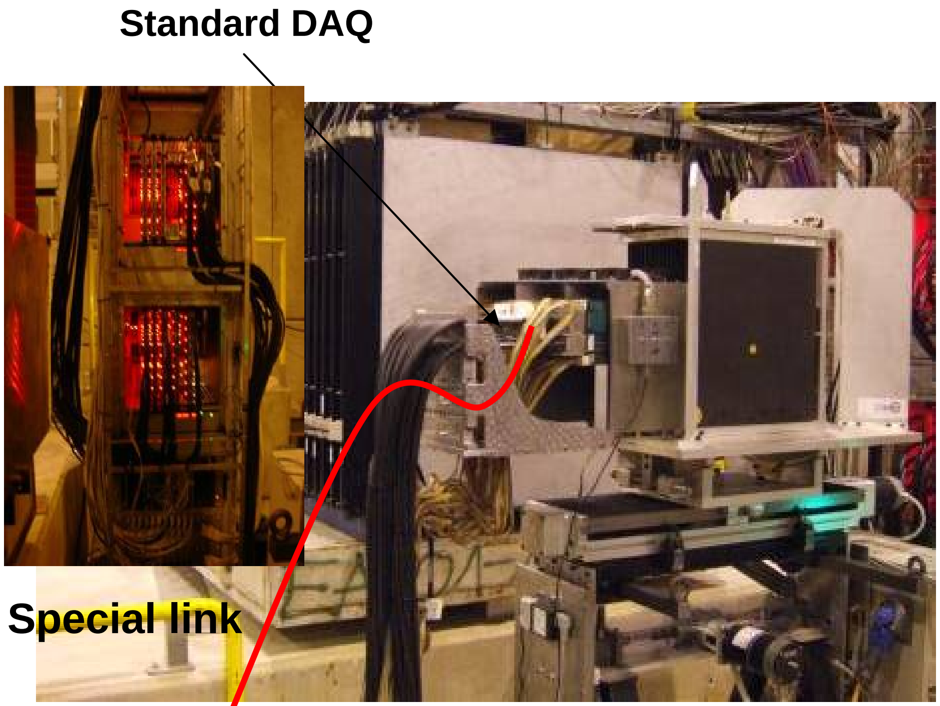
# InSituDebugDAQ
concept

**On beam** simplified **DAQ**
**devoted to monitor and debug**
a few SLABs
- chip radiation tolerance
- accurate diagnostic
of unexpected behavior
- monitoring (internal probes)
- maintenance

Can run alone, eventually with no beam
- compatible with machine interface
or **specific trigger** and timing

**Dedicated Software** aimed to ease debugging

Simultaneous DAQ operations allowed




Machine Interface Or Stand alone

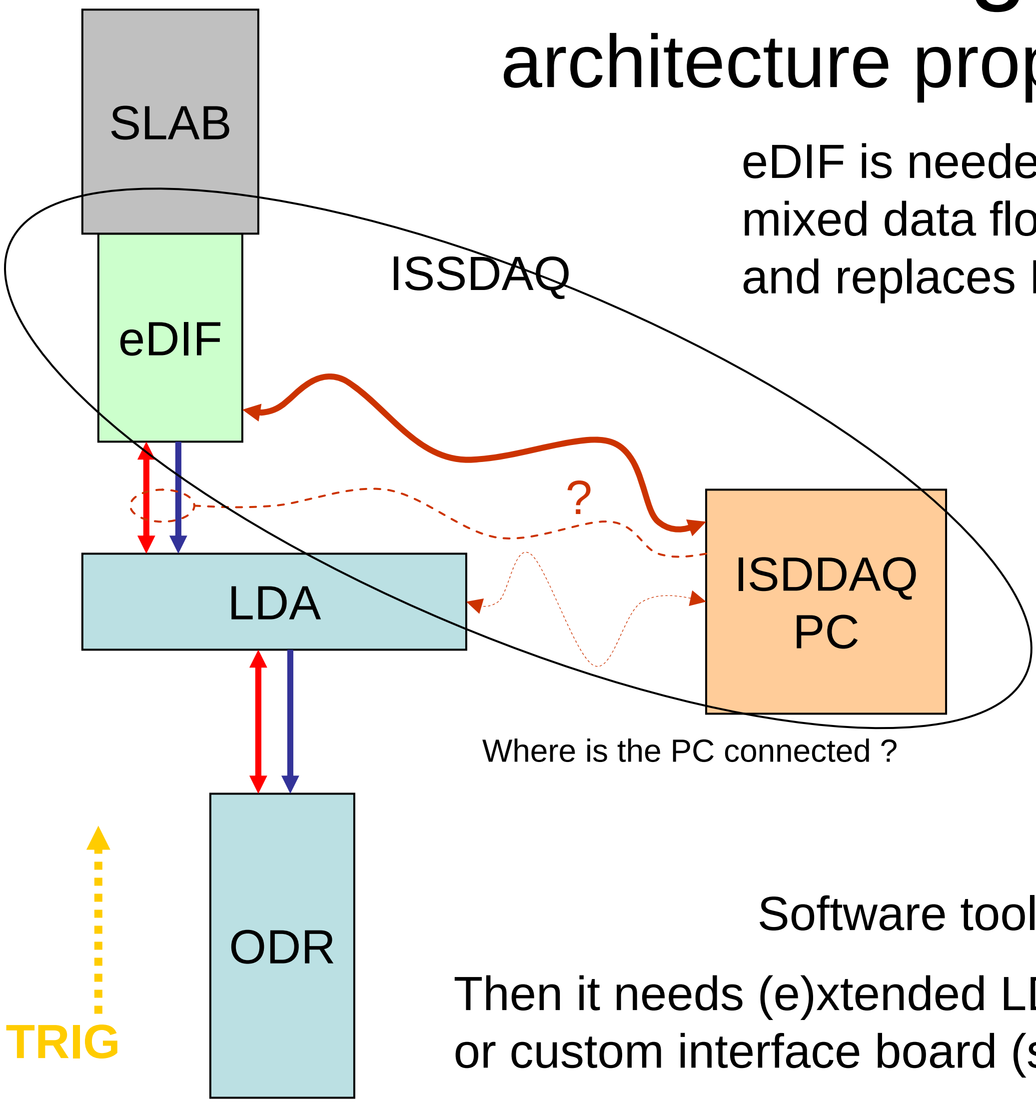
CCC

DebugDAQ

Dedicated PC

**Needs DIF** (already connected to SLAB)

# InSituDebugDAQ
## architecture proposal




eDIF is needed for VFE probes and mixed data flow mode (probe+DAQ) and replaces DIF when debugging

Direct connection to LDA would avoid risky cabling operations and highest flexibility

DAQ NI PCI-7811R ?

- FPGA based, 160 I/O to PCI
- buffer flush mode (continuous streaming to PC)

Or Ethernet

Software tools

Then it needs (e)xtended LDA… (CCC multiplexing) or custom interface board (serial LVDS to NI DAQ)

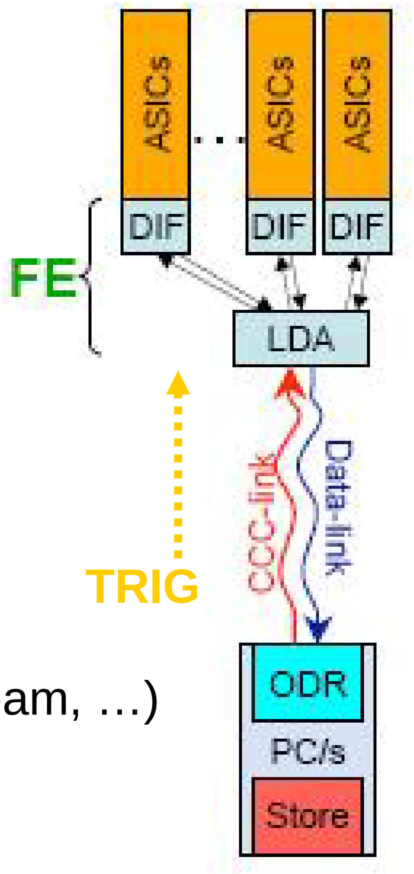
Light LDA for early devlopments

# ASU ISD DAQ vs DIF (idea)

Hard/firm/software developments for ASUDAQ & ISDDAQ are
Very similar as for DIF

ISDDAQ is a DIF with extended features and direct read-out

DIF is a light ASUDAQ,
ASUDAQ is a DIF with extended features
• slow control of internal probes
• ADC for probe output (will be integrated into VFE ?)
• probe data read-out (additional or separate flow)
• dedicated software modules

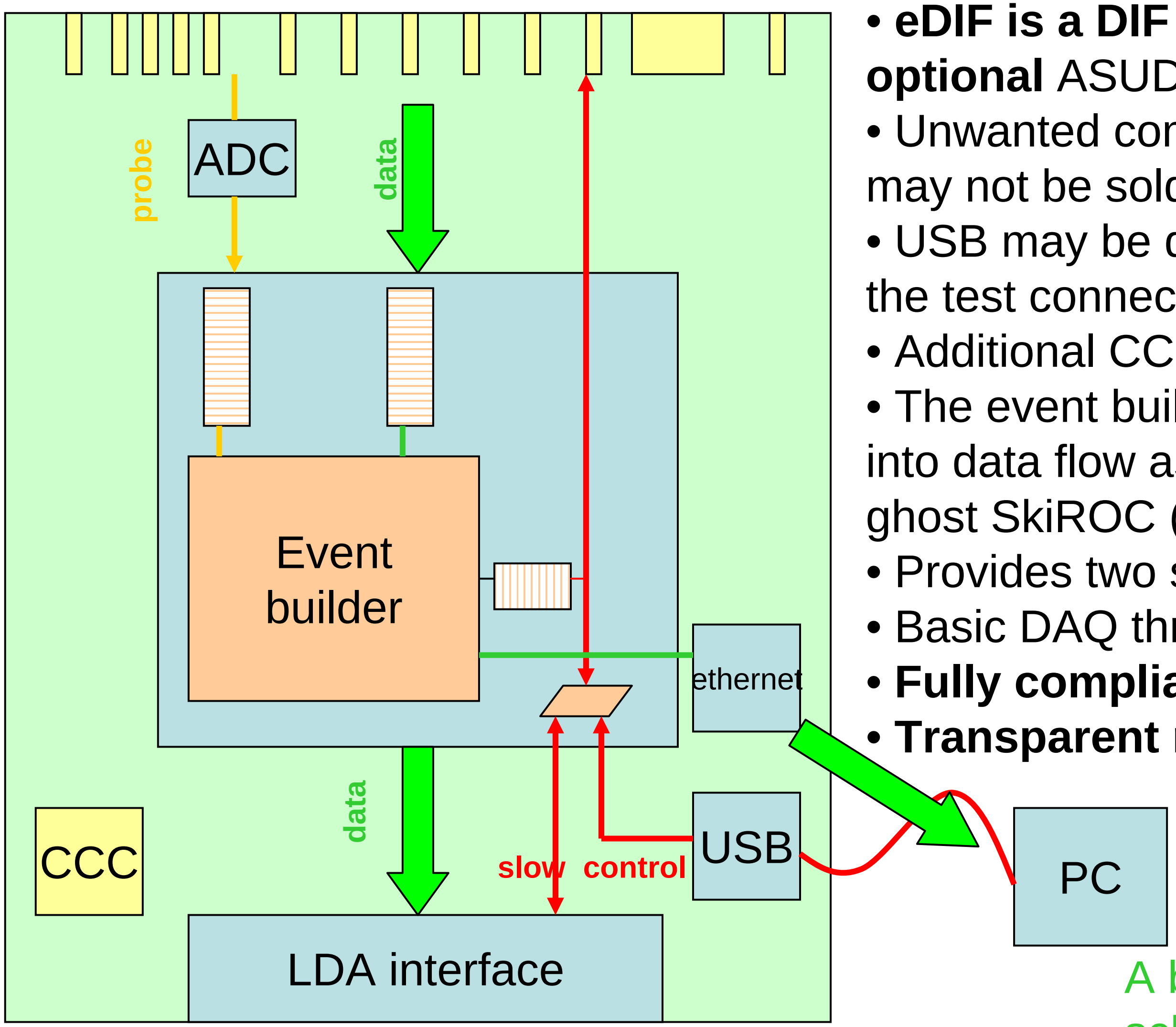



CCC additionnal signals for users defined trigger (cosmic, no beam, …)
Alternative Slow control access
Mechanical interface to ASU (ASUDAQ)

☞ **(e)xtendedDIF concept**

# eDIF proposal

## first attempt architecture




- **eDIF is a DIF** including **optional** ASUDAQ **features**
- Unwanted components may not be soldered
- USB may be deported using the test connector foreseen on DIF or on LDA
- Additional CCC signal through debug con.
- The event builder add probe data into data flow as coming from ghost SkiROC (**combined data flow mode**)
- Provides two slow control access
- Basic DAQ through USB (ASUDAQ)
- **Fully compliant with LDA** (DebugDAQ)
- **Transparent mode** (standard DAQ)

- Stand alone DAQ through Ethernet (high speed)

A board is being designed : schematic mostly done

# Conclusion

ASUDAQ and ISDDAQ need analogue signals of internal probing system to be connected to DIF

- eDIF concept
- architecture choice
- Combined data flow mode

**Wafer test bench being set up**

- PCB specifications
- Keithley choice
- Shaper
- SILVACO simulation tools

**ASUDAQ**

- first developments on prototyping board
- ASU connector issue

**ISDDAQ architecture issue**

- Internal probes
- Simultaneous DAQ
- Flexibility

**Common "all in one" prototype is being designed**

- generic interfaces
- use of additional adapter board to connect to ASU, SLAB, etc…