



# Belle 2 Upgrade Plans

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15th December 2023, IPHC

Current design images taken from the Belle 2 upgrade CDR (V2): CWR version released 12 December 2023

#### Vacant Belle 2 positions @ QMUL:

- Silicon detector tech to help work on Belle 2 upgrades (and ITk), advert out early in 2024
- Belle 2 PhD candidate to start in autumn 2024

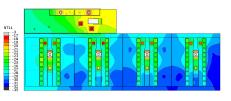


## **Background**

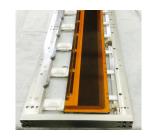
- QMUL worked with INFN Pisa and colleagues on the SuperB vertex detector design
- In parallel worked on the Arachnid CMOS MAPS project (180nm TJ) that was a precursor to the Alpide chip design that ALICE developed
- We work on the ATLAS Inner Tracker Upgrade: Strip Tracker and Pixel Endcap systems covering sensor testing, mechanical design, tooling, quality control for local supports, and simulation of radiation environments



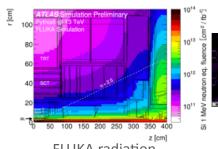
Silicon strip sensors for LHC



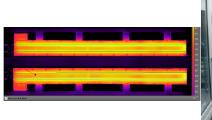
Heat transfer simulation for detector system cooling design



Module assembly engineering



FLUKA radiation environment simulations



Infra-red thermal imaging system



Fully equipped ISO 7 certified clean room





- 1. Wafer and sensor testing
- 2. Module assembly design
- 3. Layer 1 and 2 mechanics
- 4. Understanding of interface to the rest of the VTX
- 5. Next steps

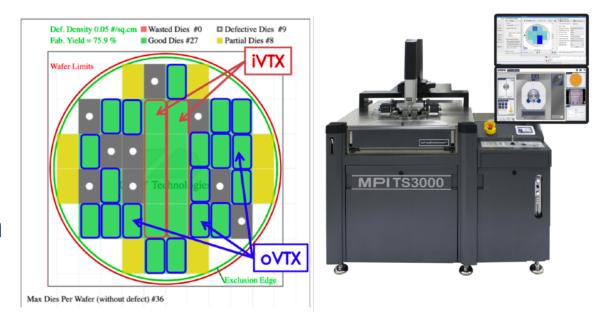
#### Our aims for today:

- Get to know people already working on the project
- Check that we are focusing on the right questions
- Making sure we work constructively with ongoing and planned efforts
- Get a better understanding of what the collaboration is already doing





- Wafer and sensor testing
- Aim to support the R&D and production in one of our cleanrooms
- Will have access to a probe station that will be dedicated for the duration of production to Belle 2
- Able to operate between -60 and 300C for testing over a range of operational conditions [dry environment]
- Will give the QM team an understanding of the chip that can help with detector design and construction.



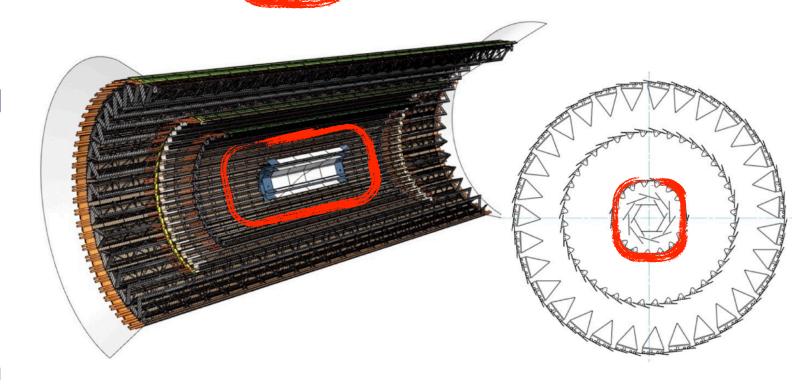
- 300 mm probe station with thermal chuck for wafer probing
- Aim to use BDAQ53 system for chip tests and wafer probing
- Finalising a Si-Det tech advert for someone to work on ITk and Belle 2





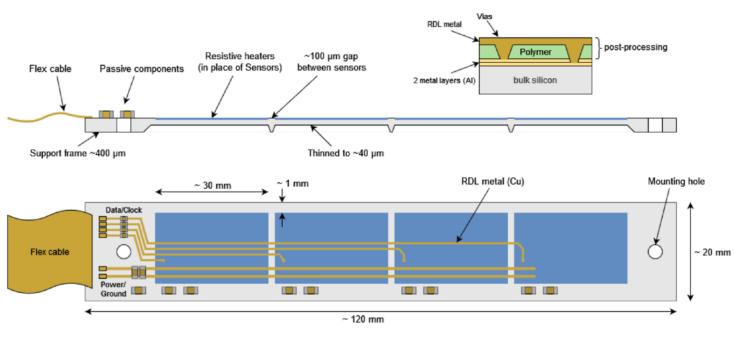
- Work on the module assembly and integration concepts for the iVTX:
  - Module design and assembly
  - Layer 1 (r=14.1mm) and Layer 2 (r=22.1mm)
- Module assembly
- Test/handling frames
- Integration into layer
- Mounting onto the system

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Layer	1	2	3a	4	5	Total	3b	Total
Radius (mm)	14.1	22.1	39.1	89.5	140.0		69.1	
# Ladders	6	10	17	40	31	104	30	117
# Sensors/ladder	4	4	7	16	$2 \times 24$	2311	12	2552
Mat. budget (% $X_0$ )	0.1	0.1	0.3	0.5	0.8	1.8	0.4	1.9





Work on the module assembly and integration concepts for the iVTX:

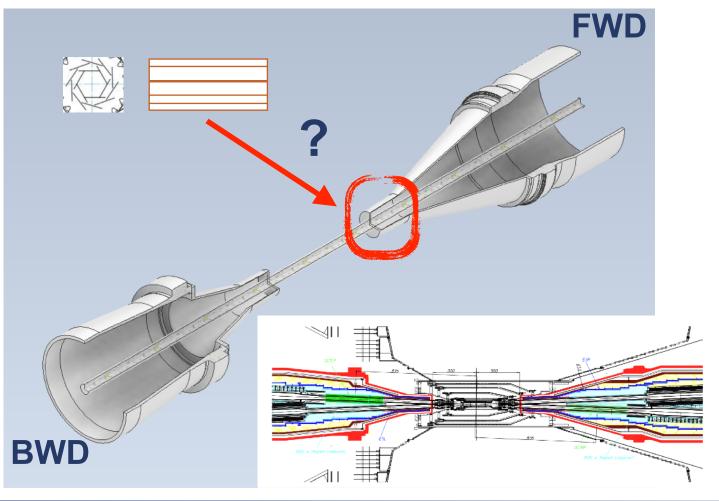


- Module assembly
- Interconnect procedure (wirebonding)
- Module handling/ shipping
- iVTX support scheme
- Integration onto support
- Mounting on structure
- Use the same solution for Layer 1 and Layer 2 modules





Understanding of interface to the rest of the VTX



- Mounting onto the forward magnet envelope
  - Fixation
  - Mechanical properties
  - Stability
  - Service interface etc.
  - Interface to the oVTX

Dominic's solid model derived from KEK's current "working" design of the QCS magnet system, likely to change - but good envelope to use as starting constraint



#### **Next steps**

- Depending on feedback from colleagues today we intend to
  - Generate an iVTX sensor model as a module model proxy (concept)
  - Use this to start to explore:
    - Storage box solutions (concept)
    - Discuss with design team about wire bond locations to inform wire bond tool requirements and wire bond tooling concept
  - Relevant deadlines in Q1 2024:
    - B2GM: Starts 29th Jan good chance to get feedback
    - STFC Belle 2 experiment submission deadline 7th Feb
    - STFC Consolidated grant submission deadline 21st Feb

UK block funding for generic R&D and running experiment M&O/travel



