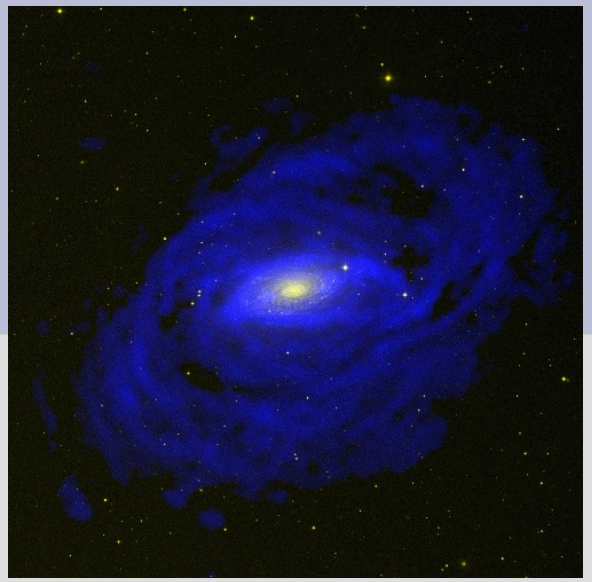
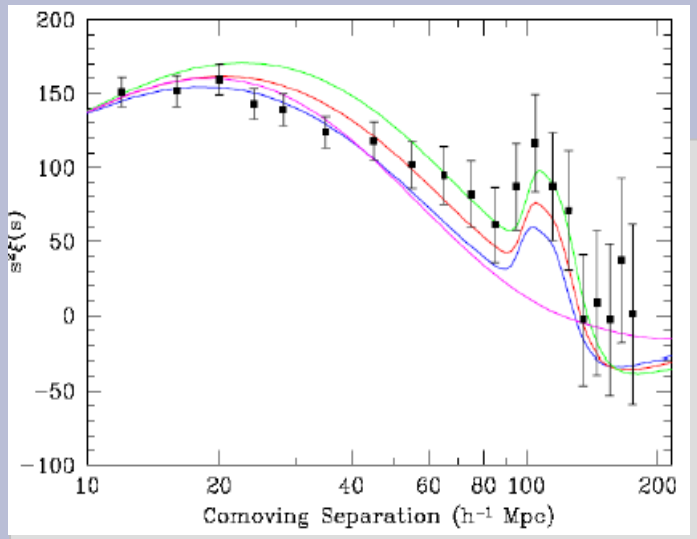
BAO radio

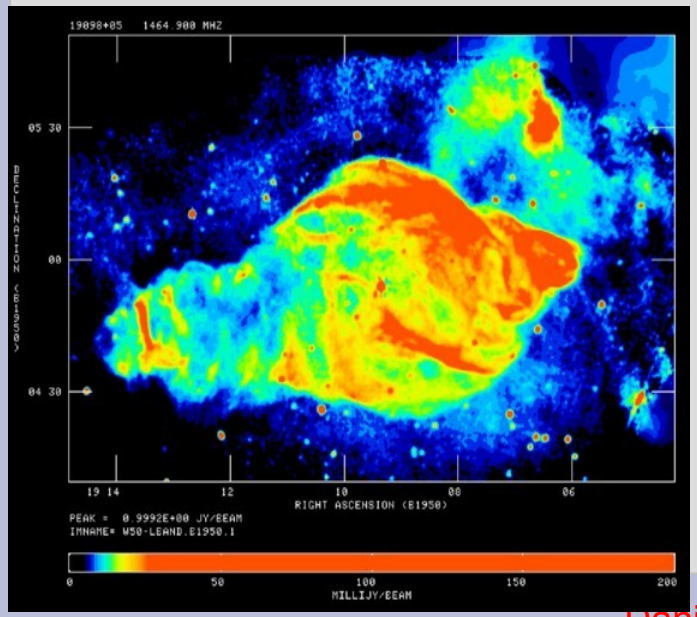


Système d'acquisition rapide pour un radio télescope multiple-voies

CEA/Irfu IN2P3/LAL CMU Fermilab colaboration

BAO : Baryonic Acoustic Oscillations





- Imprints left by the baryon-photon fluid (before recombination) in the distribution of ordinary (baryonic) matter

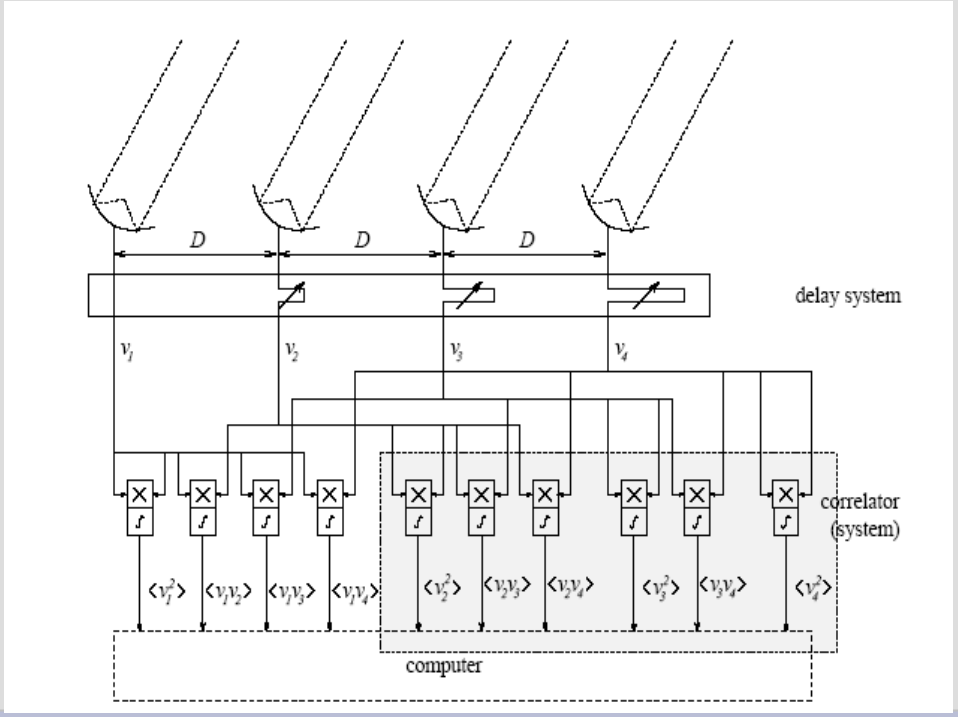
- Slight modulation of the distribution of matter, (and galaxies as tracers). Structure formation being mainly driven by CDM which dominates structure formation

- In Radio : Use 21 cm HI emission
- 3D HI mass distribution measurement through total 21 cm emission intensity mapping (No individual galaxy detection)
- Hyperfine transition (spin-orbit) of atomic hydrogen: $\nu \approx 1{,}420405$ GHz $\rightarrow \lambda \approx 21$ cm

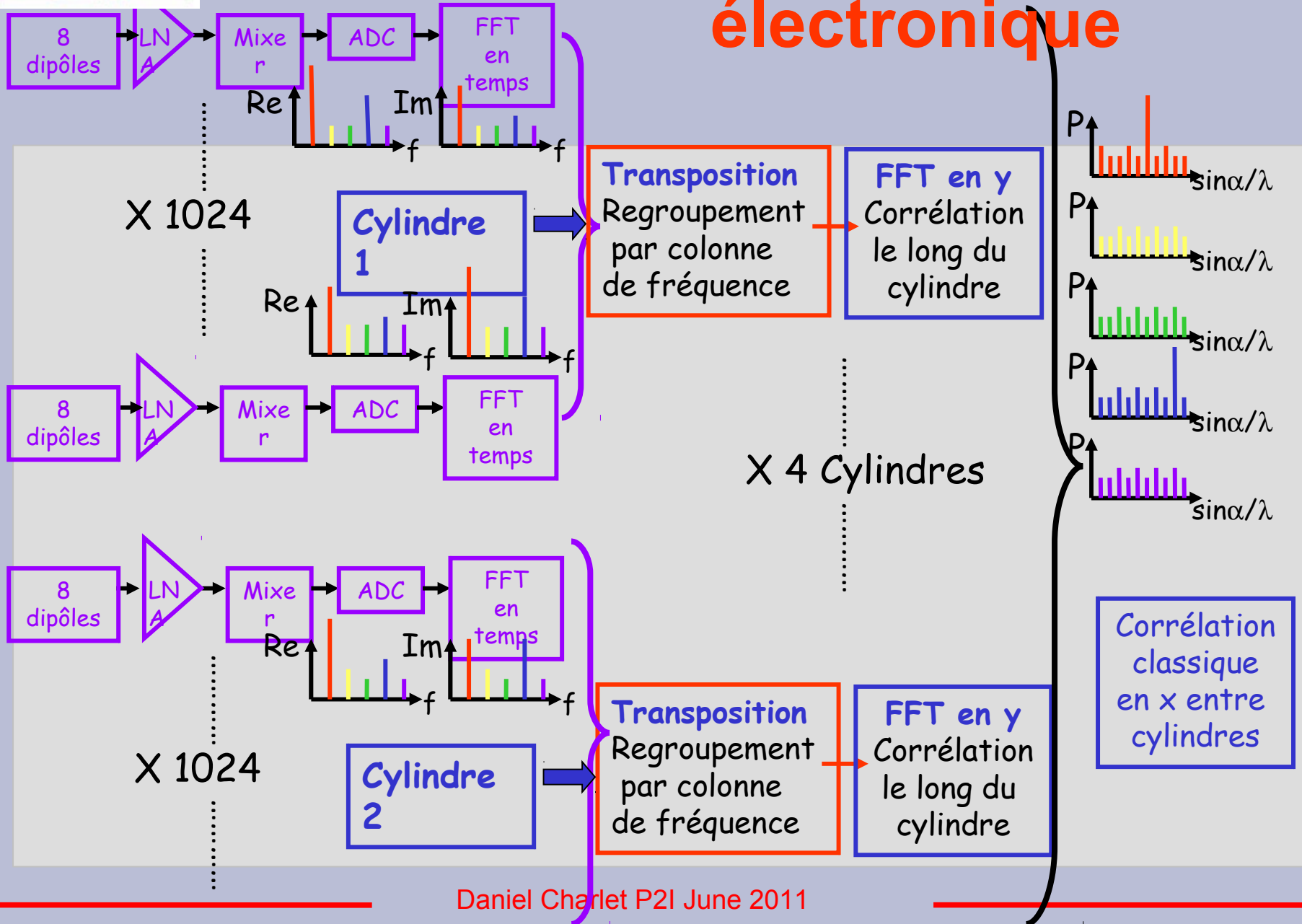
Concept: Interféromètre numérique

- Large field of view (10-100 deg^2)
- ≥ 1000 simultaneous lobes → Digital interferometer
- Wide band receivers 250 MHz
- Digital interferometer (correlator / beam-former)
- Resolution 10 arcmin, Surface ≥ 10 000 m^2
- Reflectors over an area of ~ 1000-2000 m × 1000-2000 m
- Cylindrical Radio Telescope concept or dish
- 256-512 electronic channel
- 4 bands of 250Mhz between 0.5-1.5GHz
- Sampling at 500MHz
- Possible implantation in China

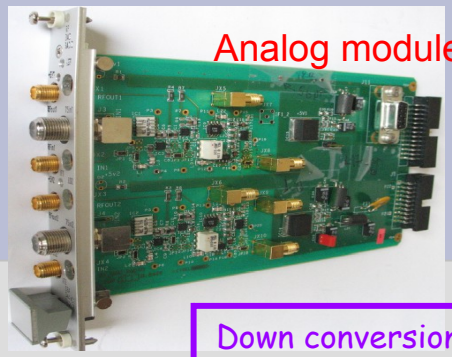
Array and corrélation

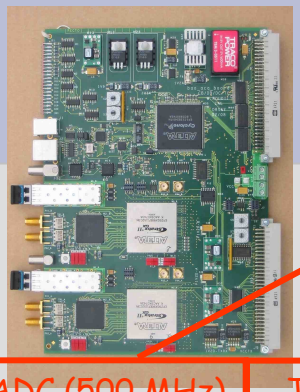


Schématique de la chaîne électronique



Chaîne électronique





X 4

Down conversion filtering

2nd

2x4Gbit/s

PC

Antenna board 4 dipoles

128 dipoles

X 4

Antenna board 4 dipoles

X 4

Down conversion filtering

2nd

ADC (500 MHz) 4 channels

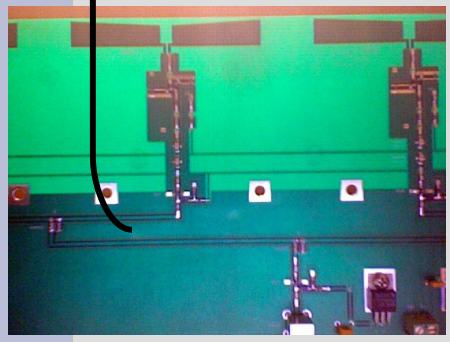
Time FFT FPGA

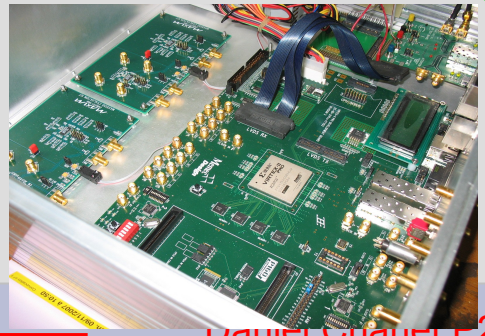
2x4 Gbit/s

Spatial FFT (FPGA)

X 8

Clock distribution





ADC (500MHz) 4 channels

Time FFT FPGA

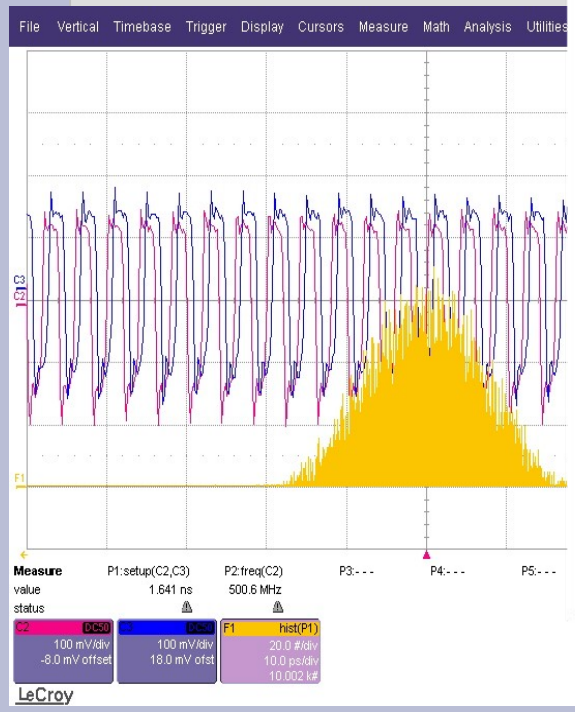
2x4.Gbit/s

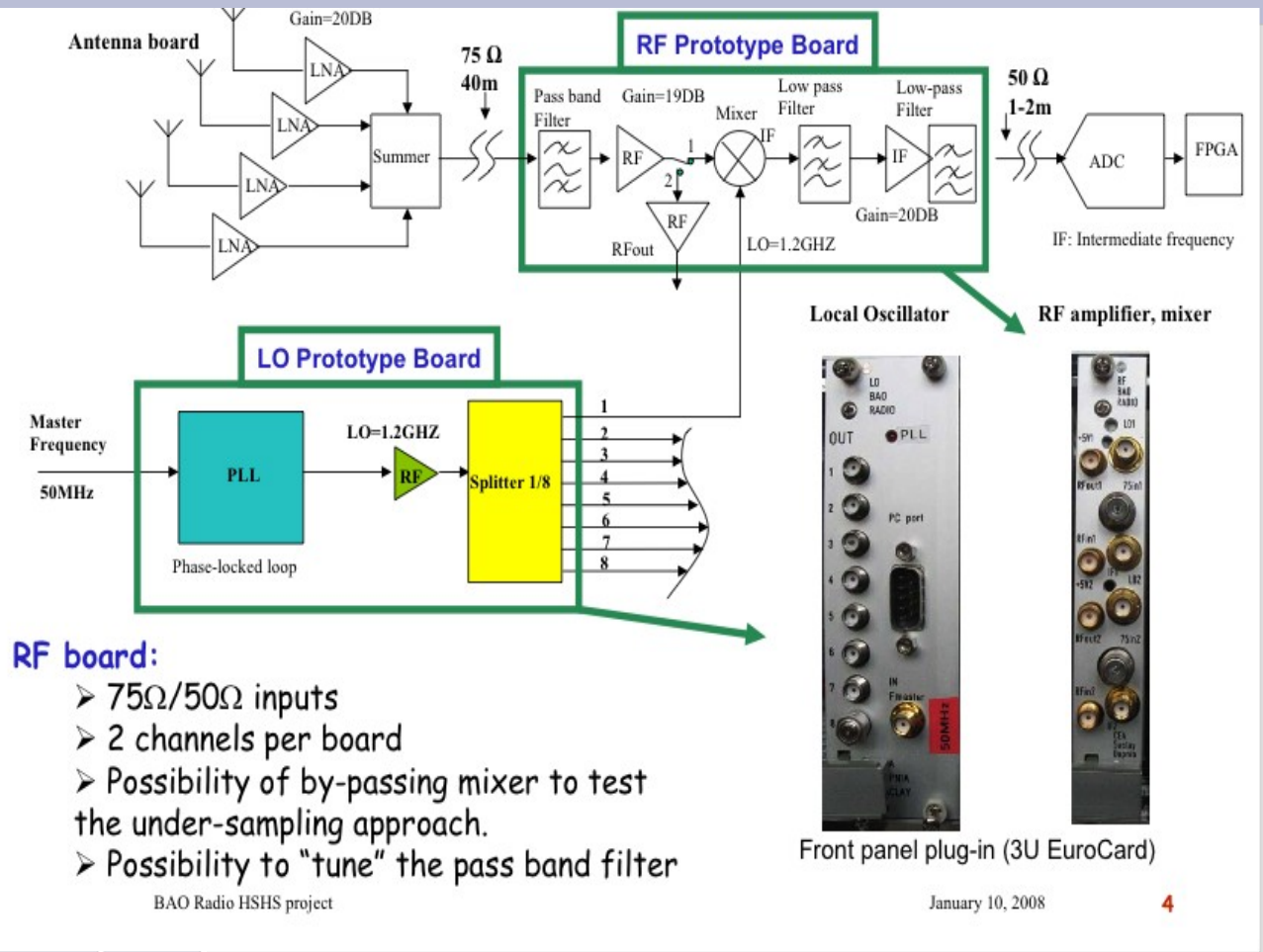
2x4 Gbit/s

PC

Chaîne analogique prototype RF

CEA irfu

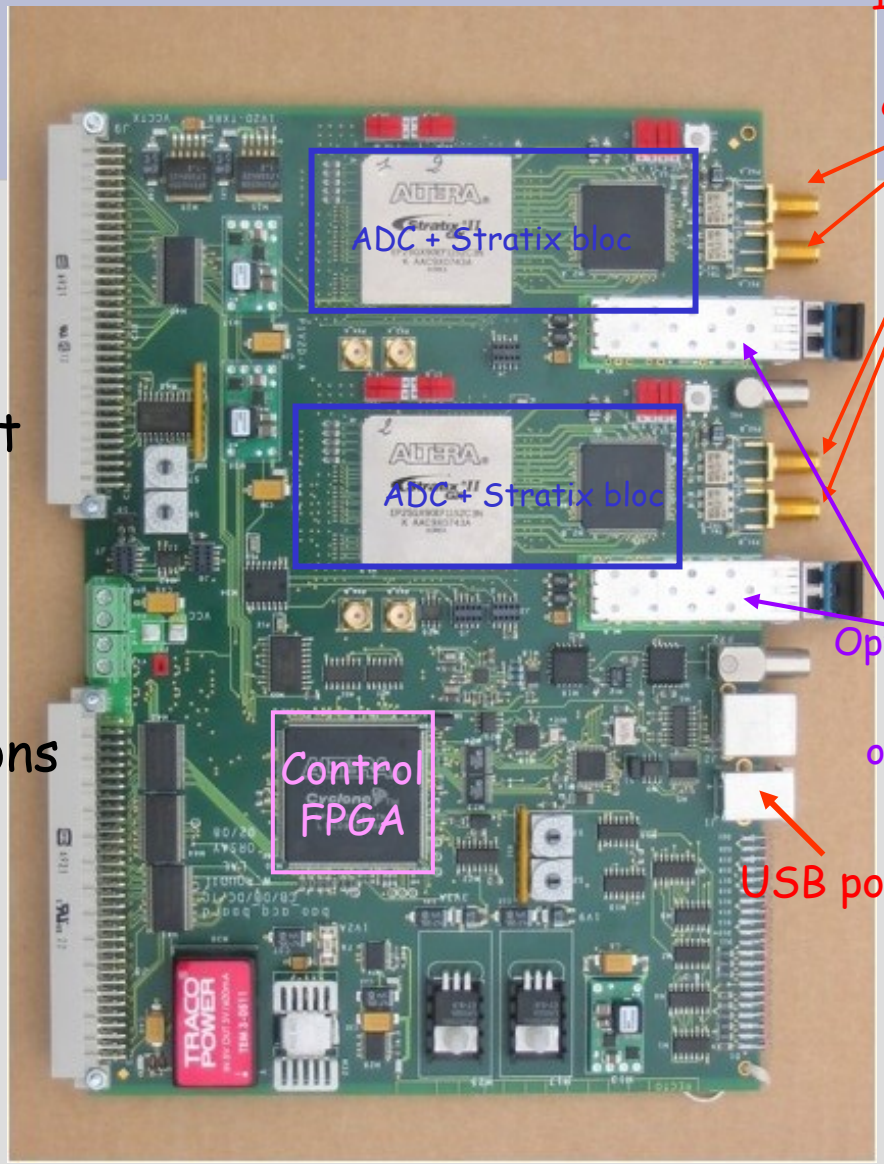




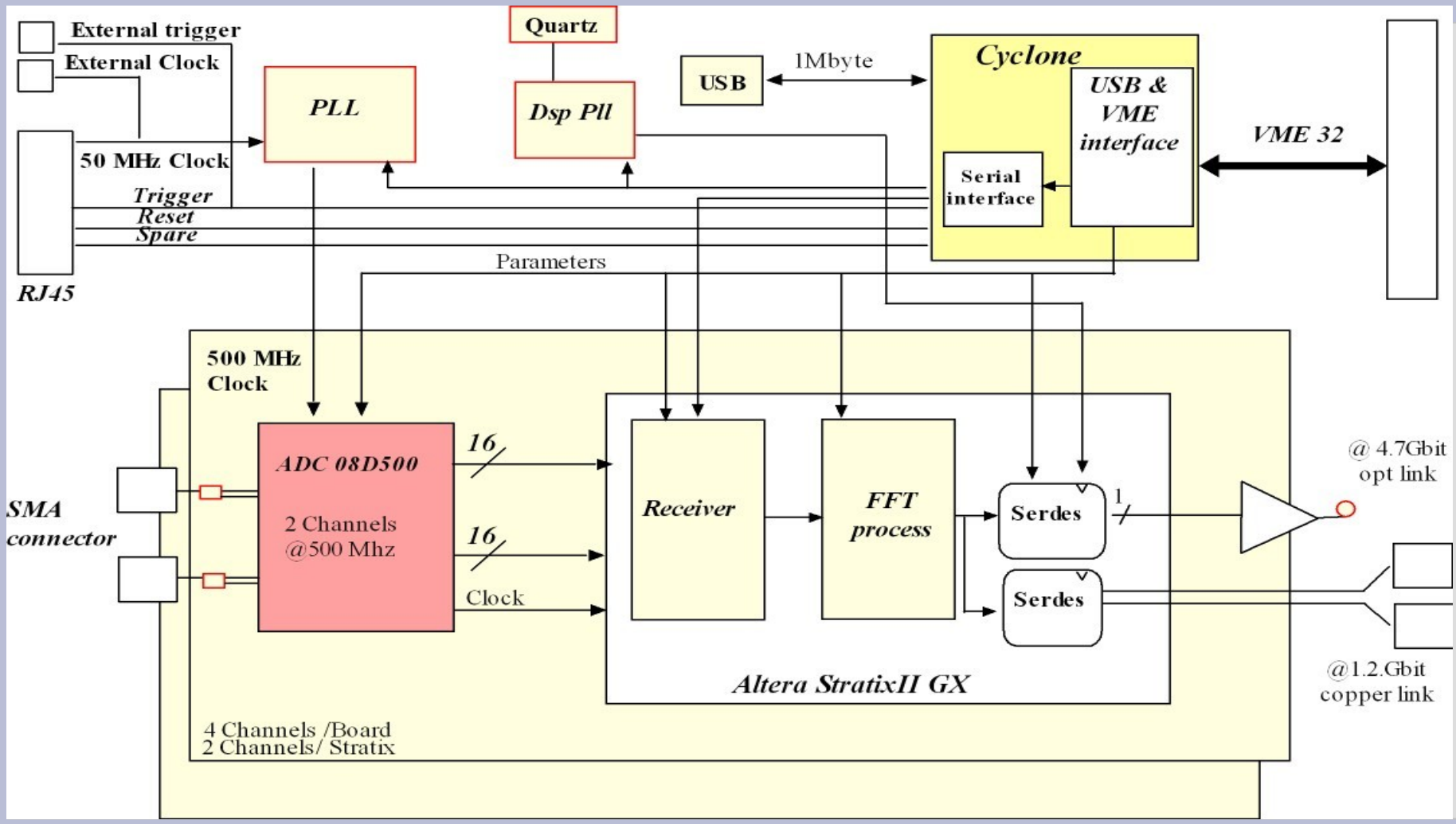
Carte ADC 500MHz

Each ADC board has :

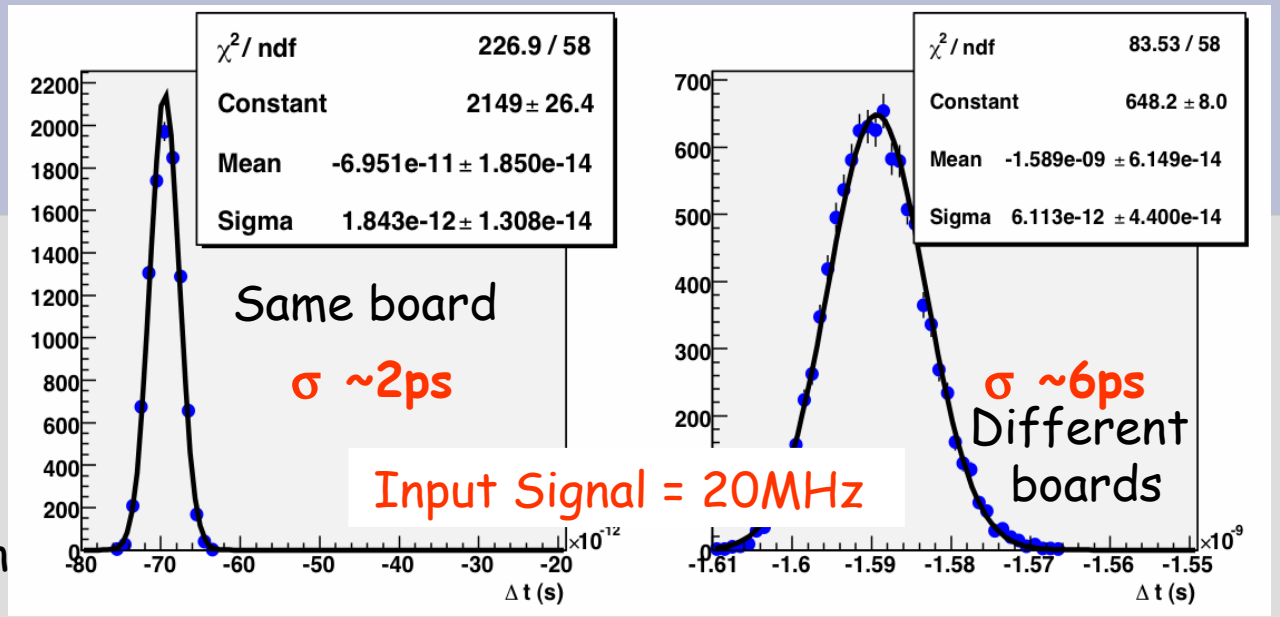
- 4 input channels (digitized at 500 MHz max)
- Input clock + control (start/stop…) ports
- USB, and VME communications port (for control)
- 2 high speed (4.8 Gbit/s) optical outputs (data links to PCI-express boards)

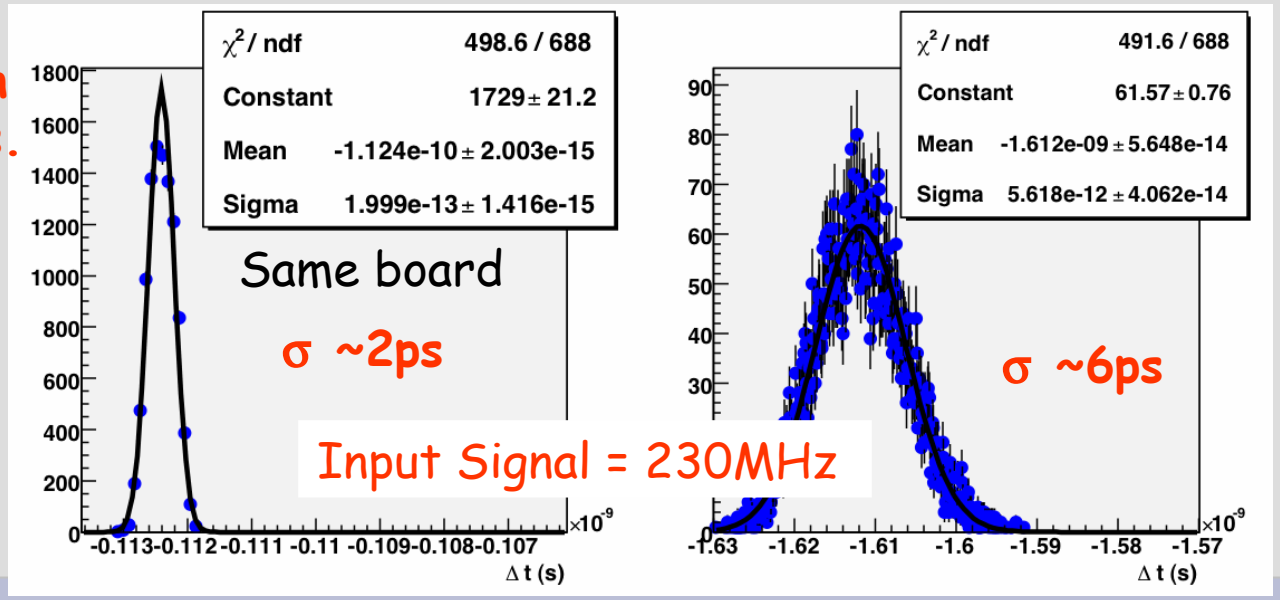


Synoptique carte ADC



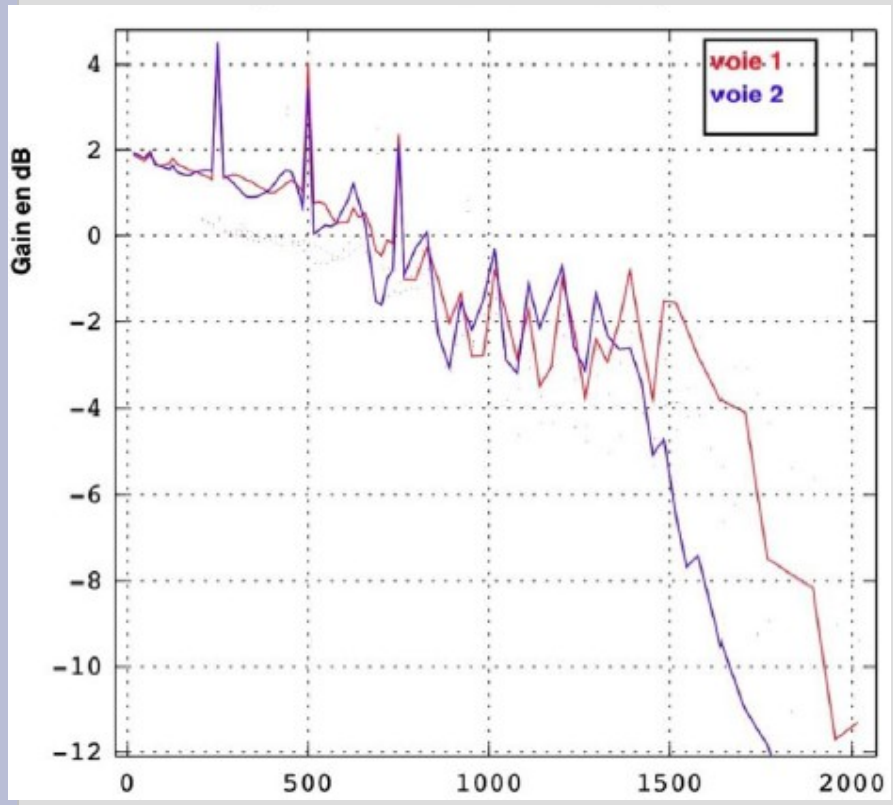
- Lot of work on pll used in ADC board to get a stable 500 MHz clock.
- **Time resolution between channel better than 10 ps.**



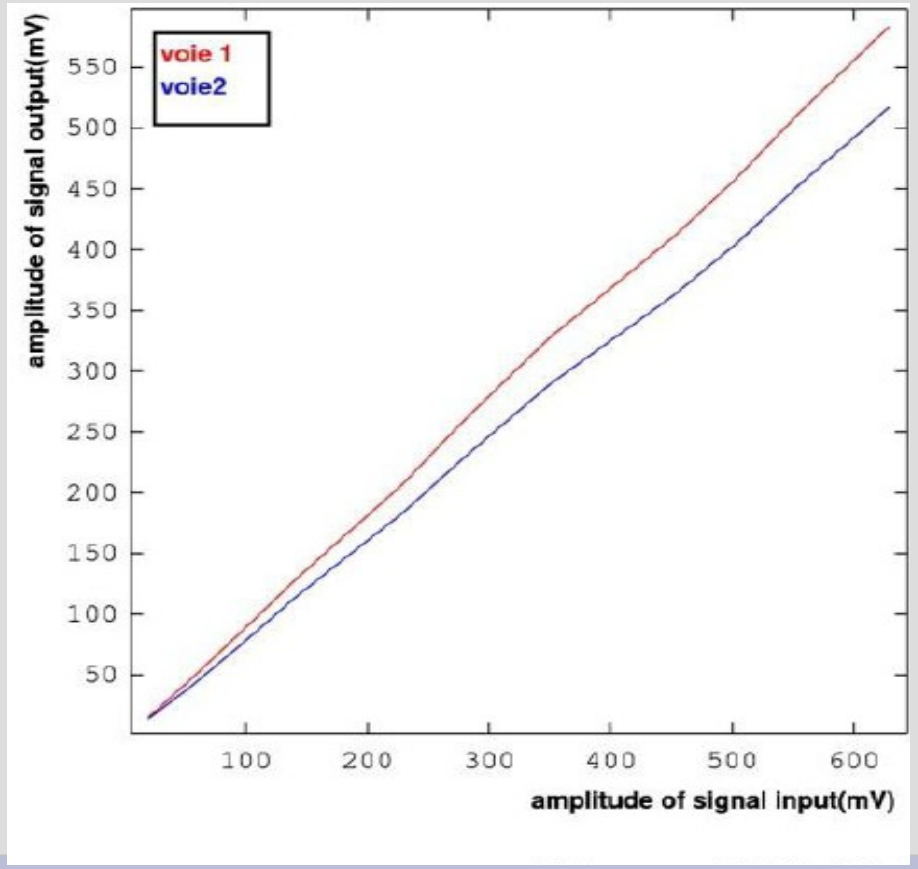


Caractéristique analogique

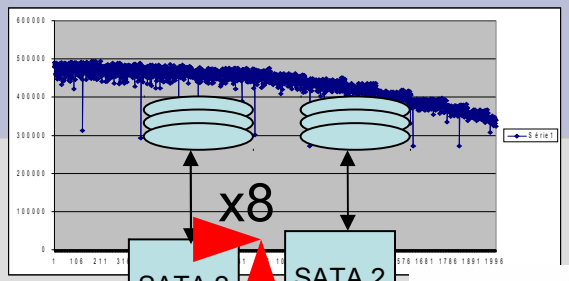
Bode diagram



Linearity at 1.4GHz



Test système acquisition



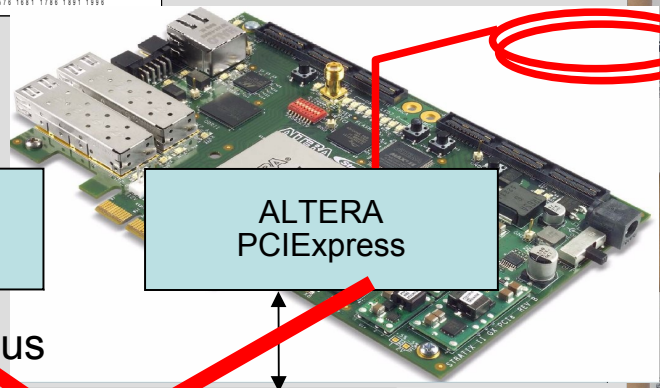
x8

SATA 2

SATA 2

PERC 5I Controller PCIX

PCIX bus



ALTERA PCIExpress

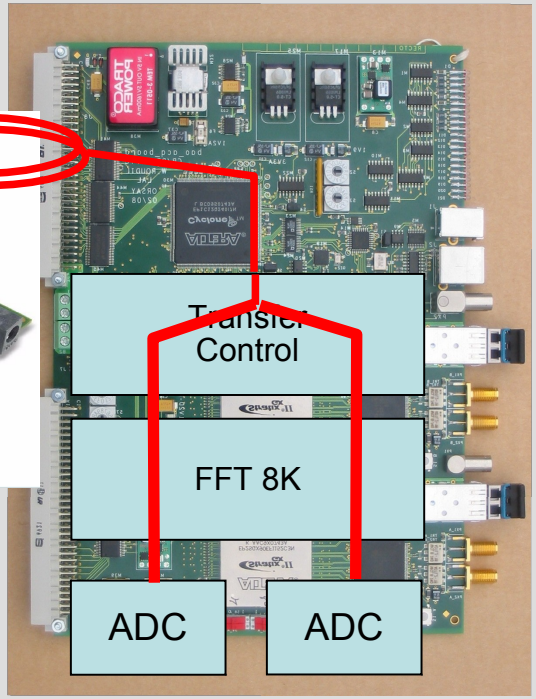
South bridge

North bridge

CPU

FSB 2000MB/s

Ram



Transfer Control

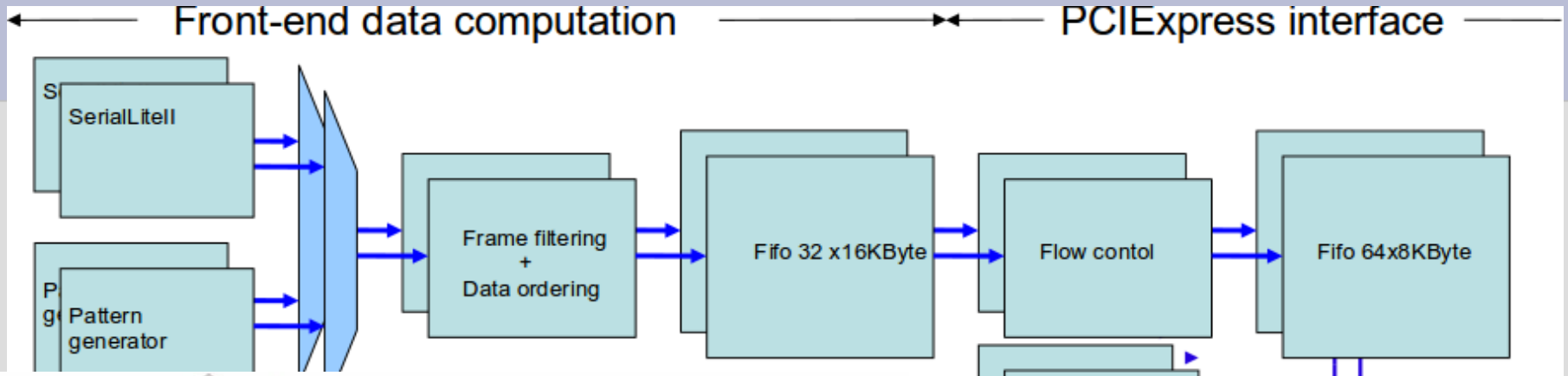
FFT 8K

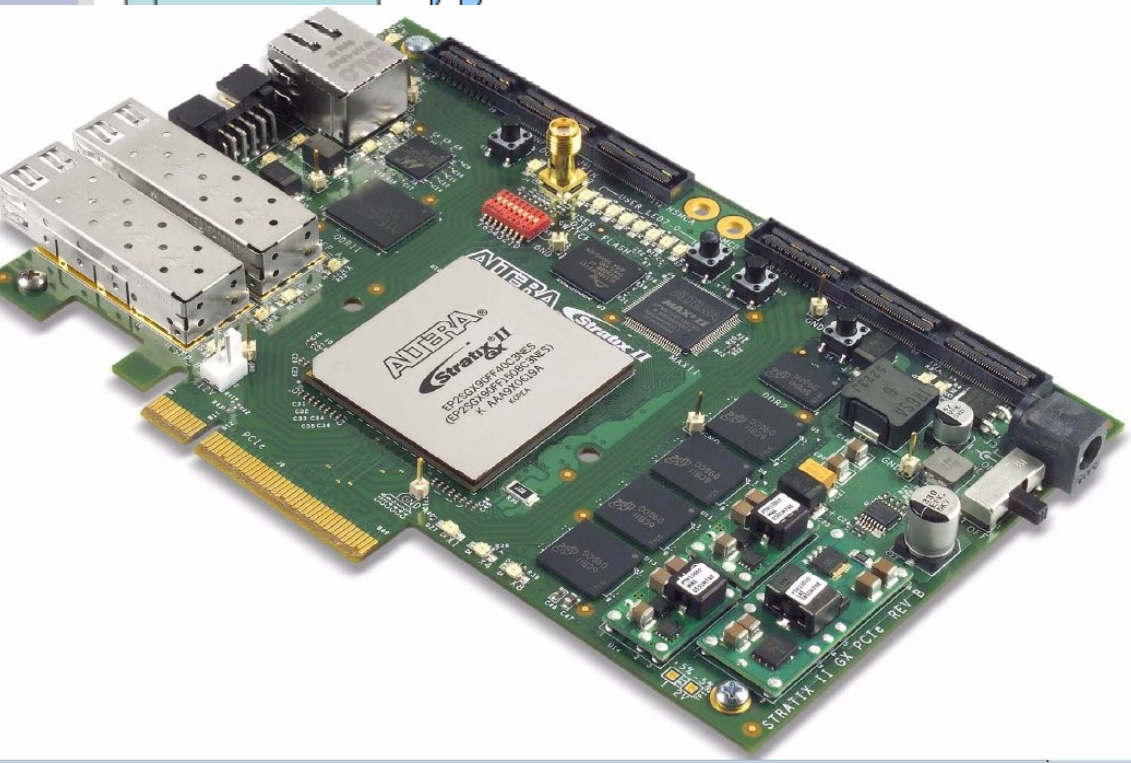
ADC

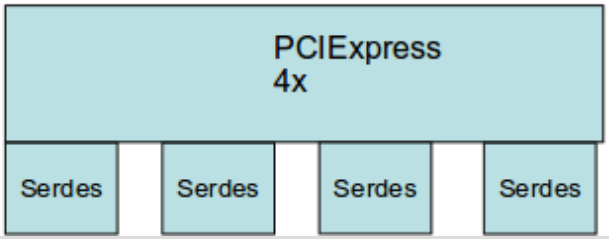
ADC

- DMA transfer
- Disk writing
- Cpu treatment
- Multi hardware tested
- Multi OS tested

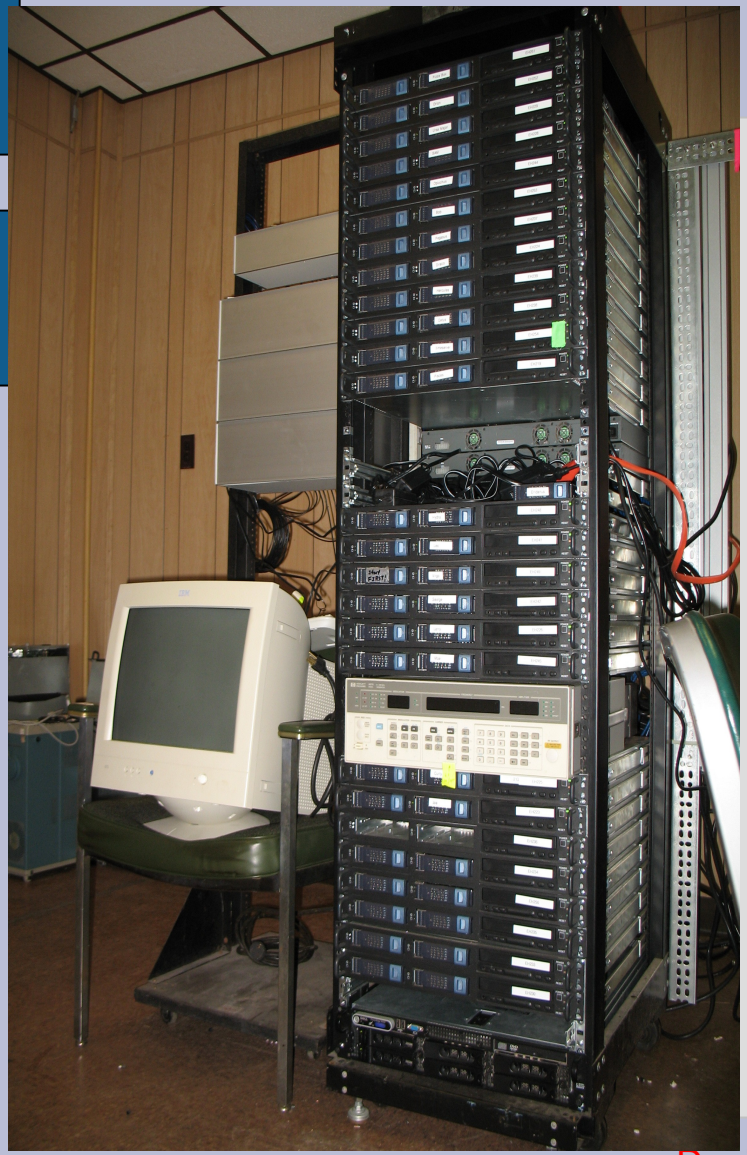
PCIExpress: carte évaluation

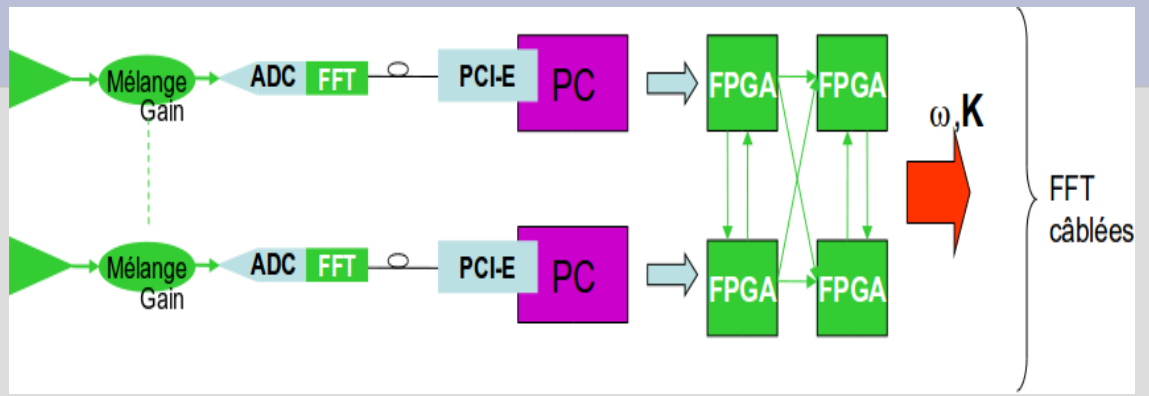


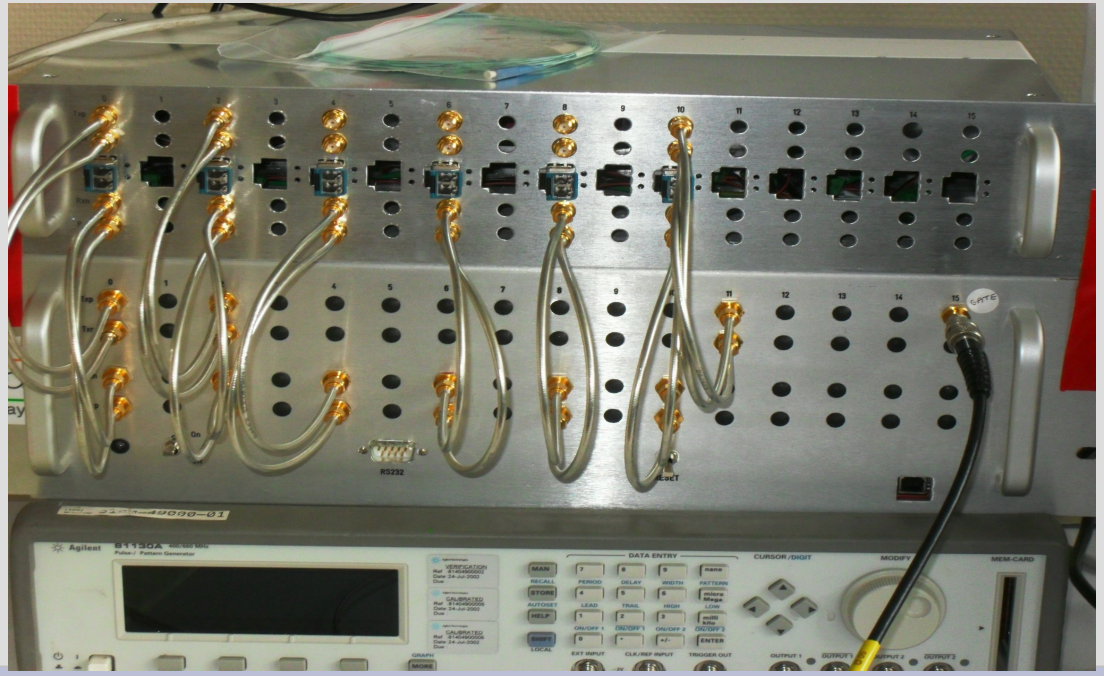




Corrélateur







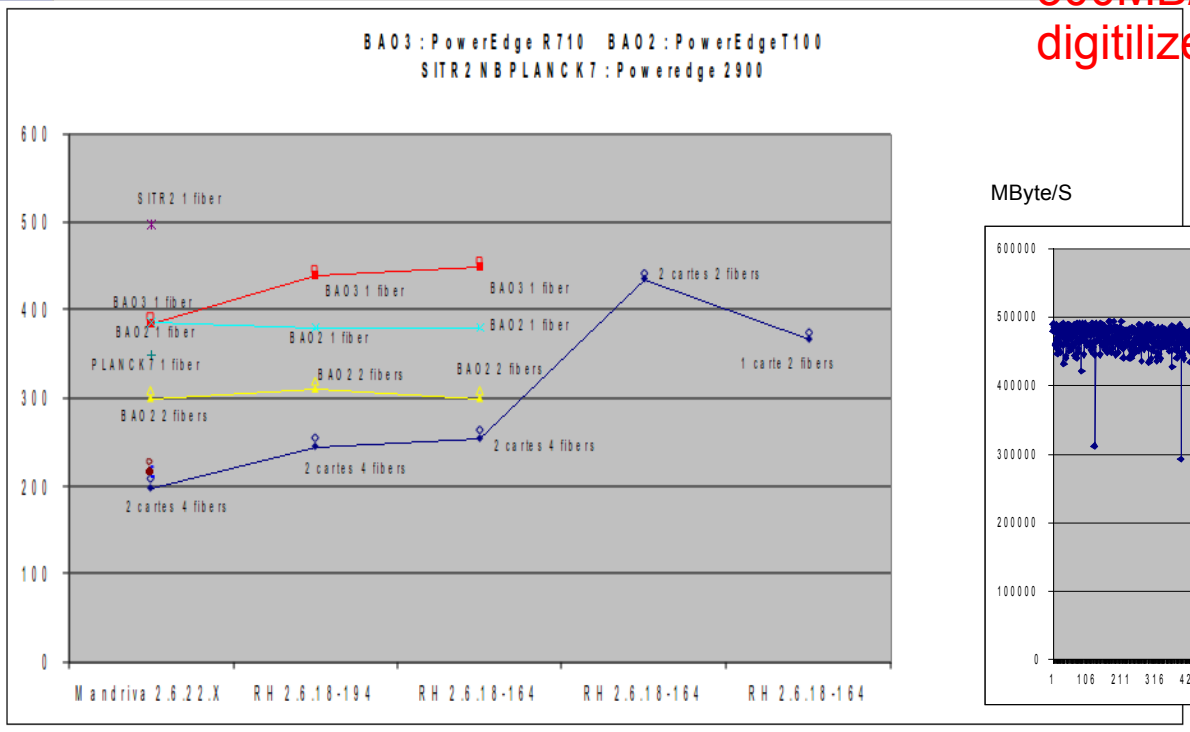
Transfert des donnés sur PC

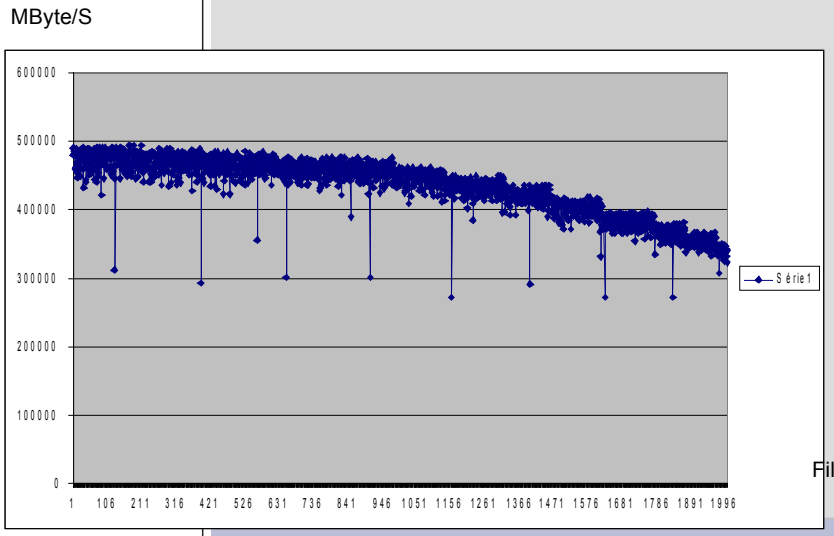
Multi-thread acquisition software:
- PCIExpress DMA
- Disck write

PCIEpress DMA transfert :

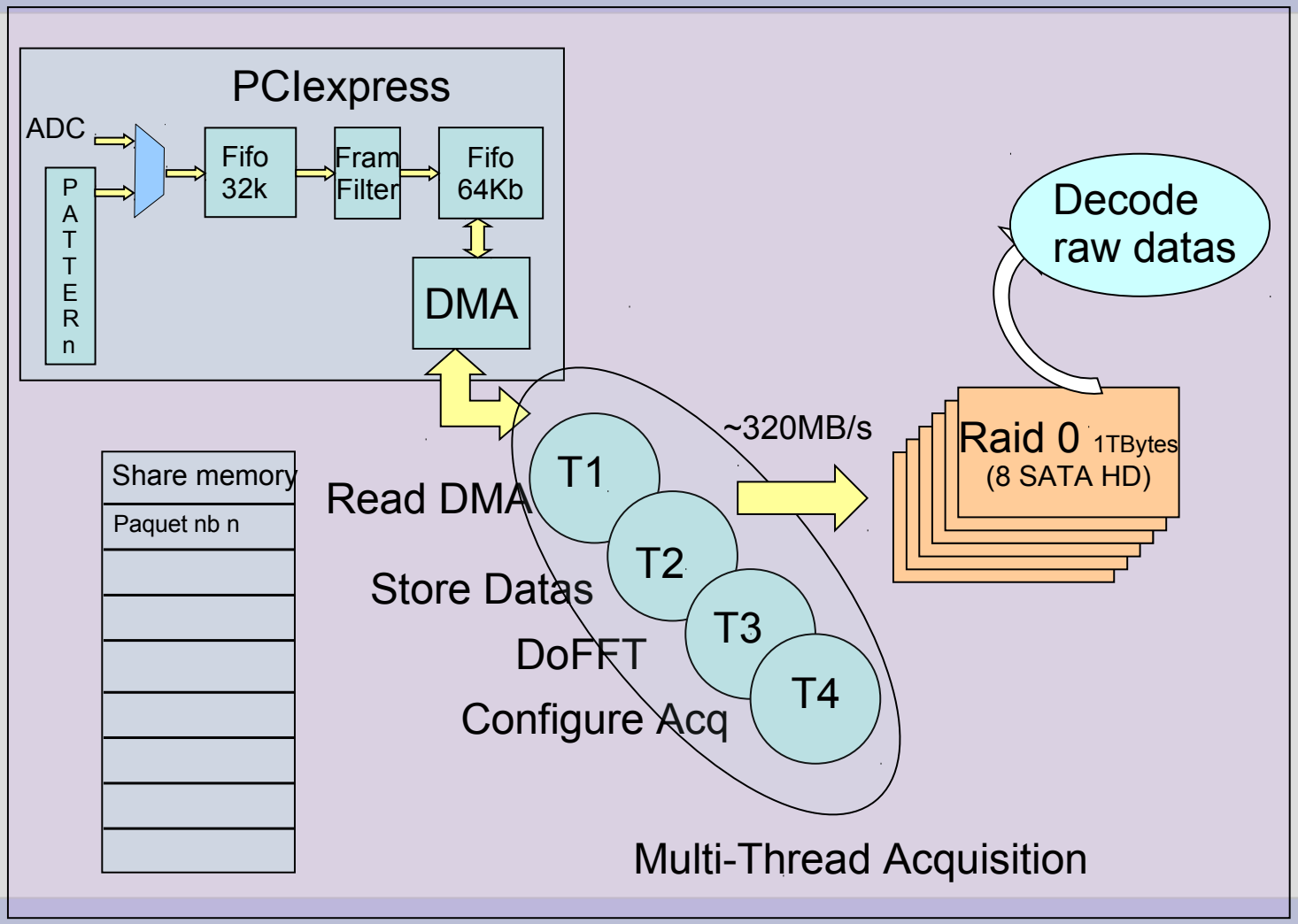
Average throughput 430MB/s

300MB/s substained data rate from digitilizer to PC-disck

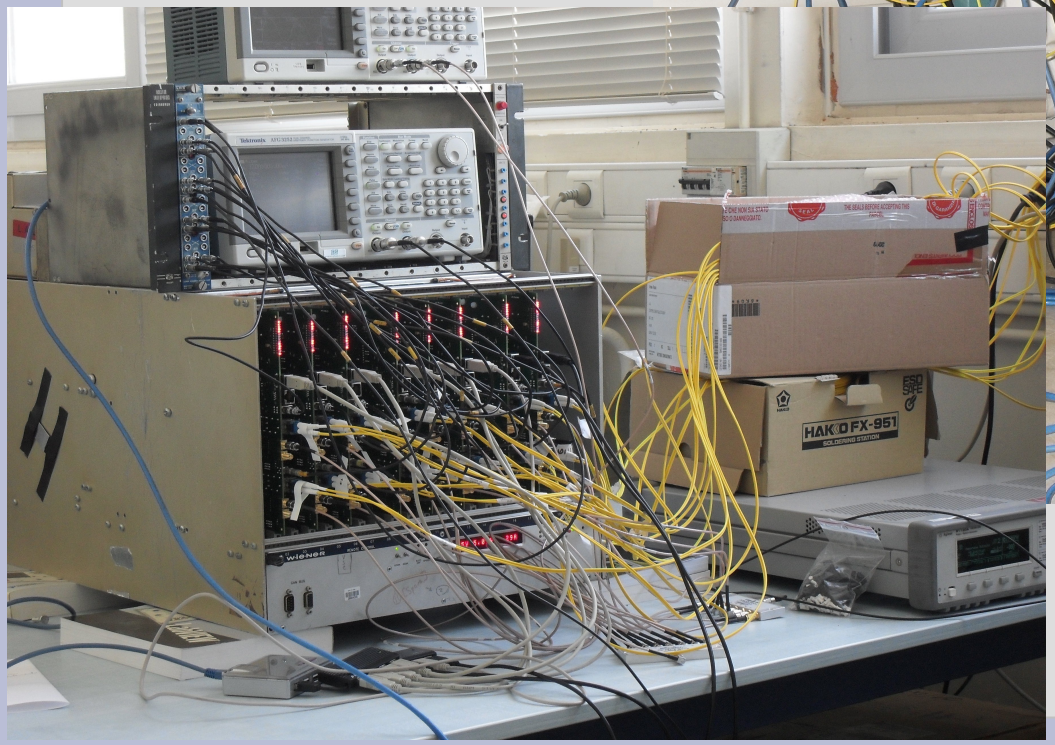




Acquisition des données

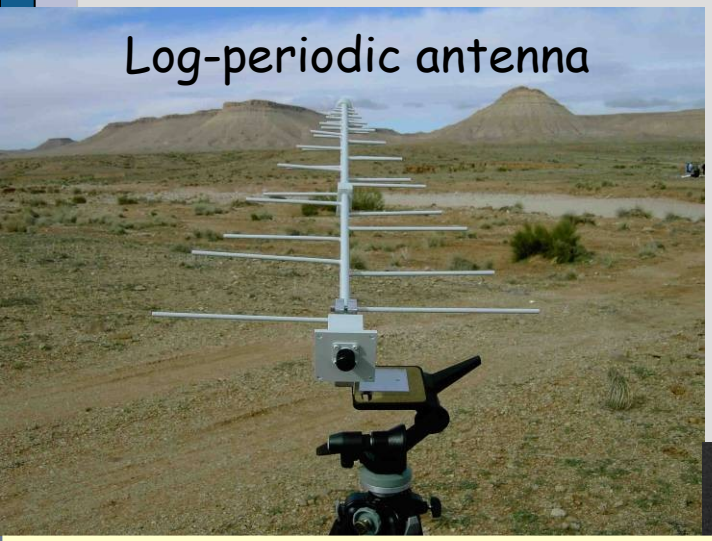


Système acquisition prototype

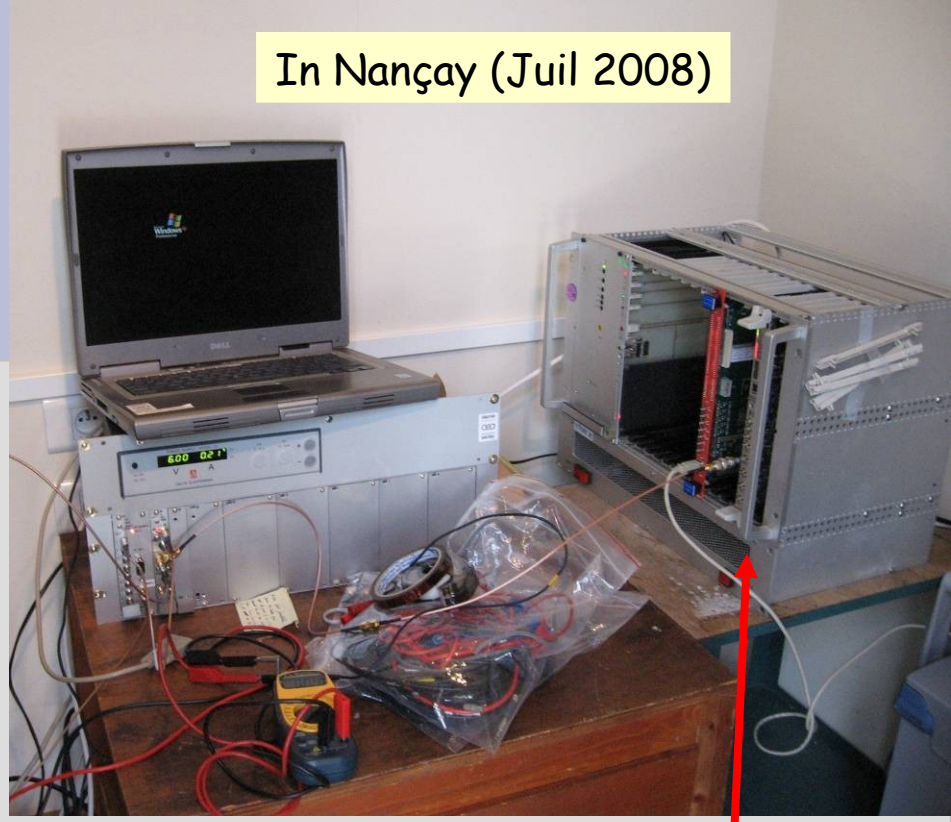


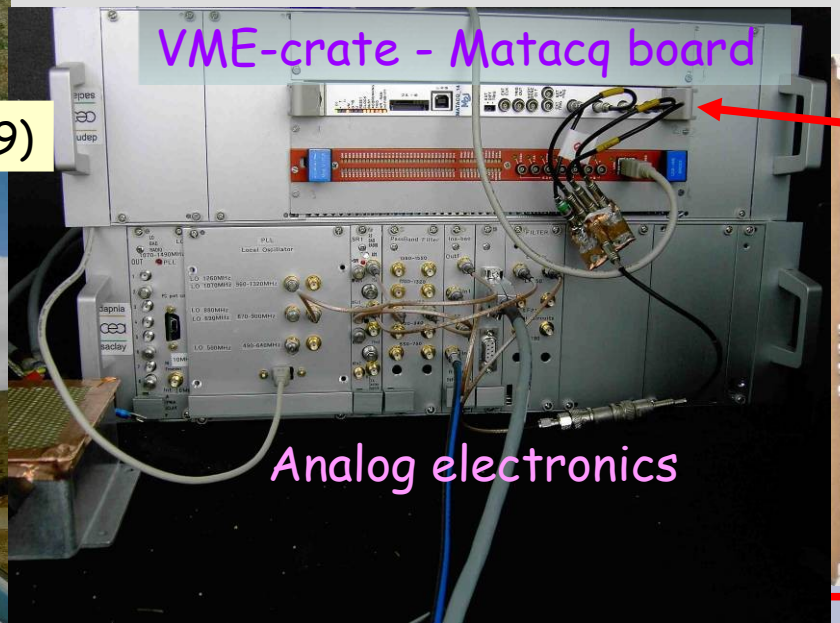
Système expérimental

Before BAO_ADC board was ready, acquisition was based on Matacq14 board



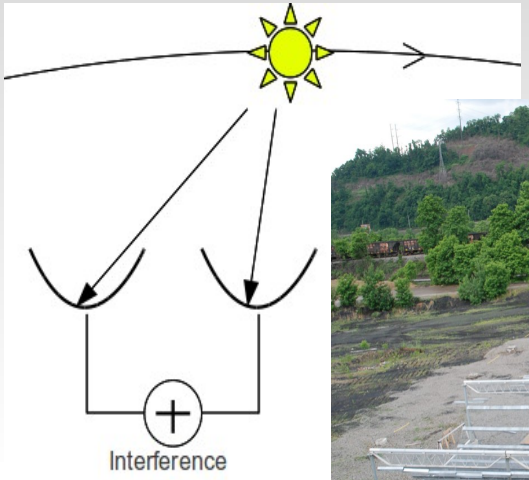
In the Morrocan desert (Jan 2009)



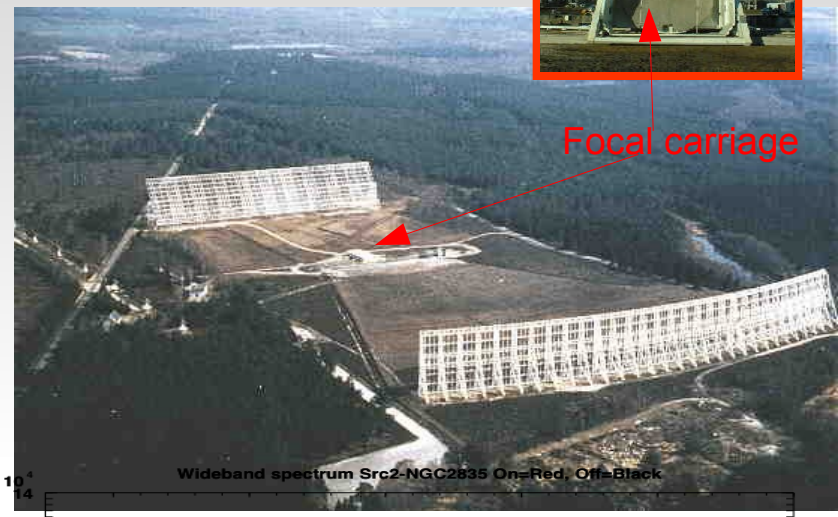


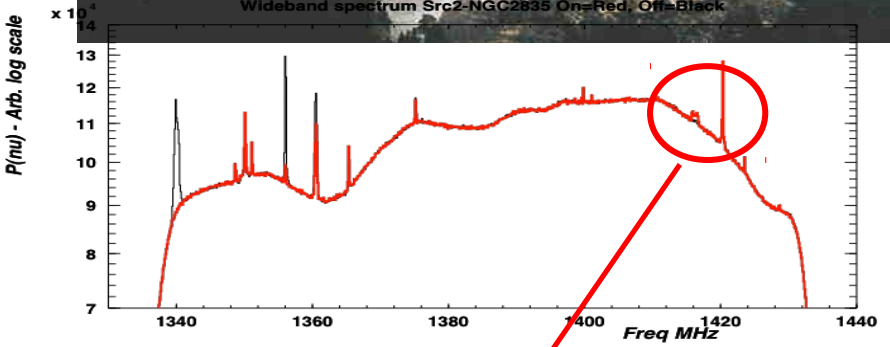
Test sur site

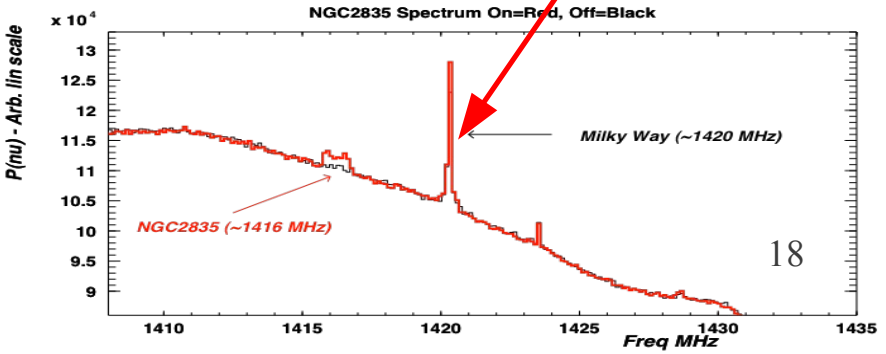
Pittsburgh



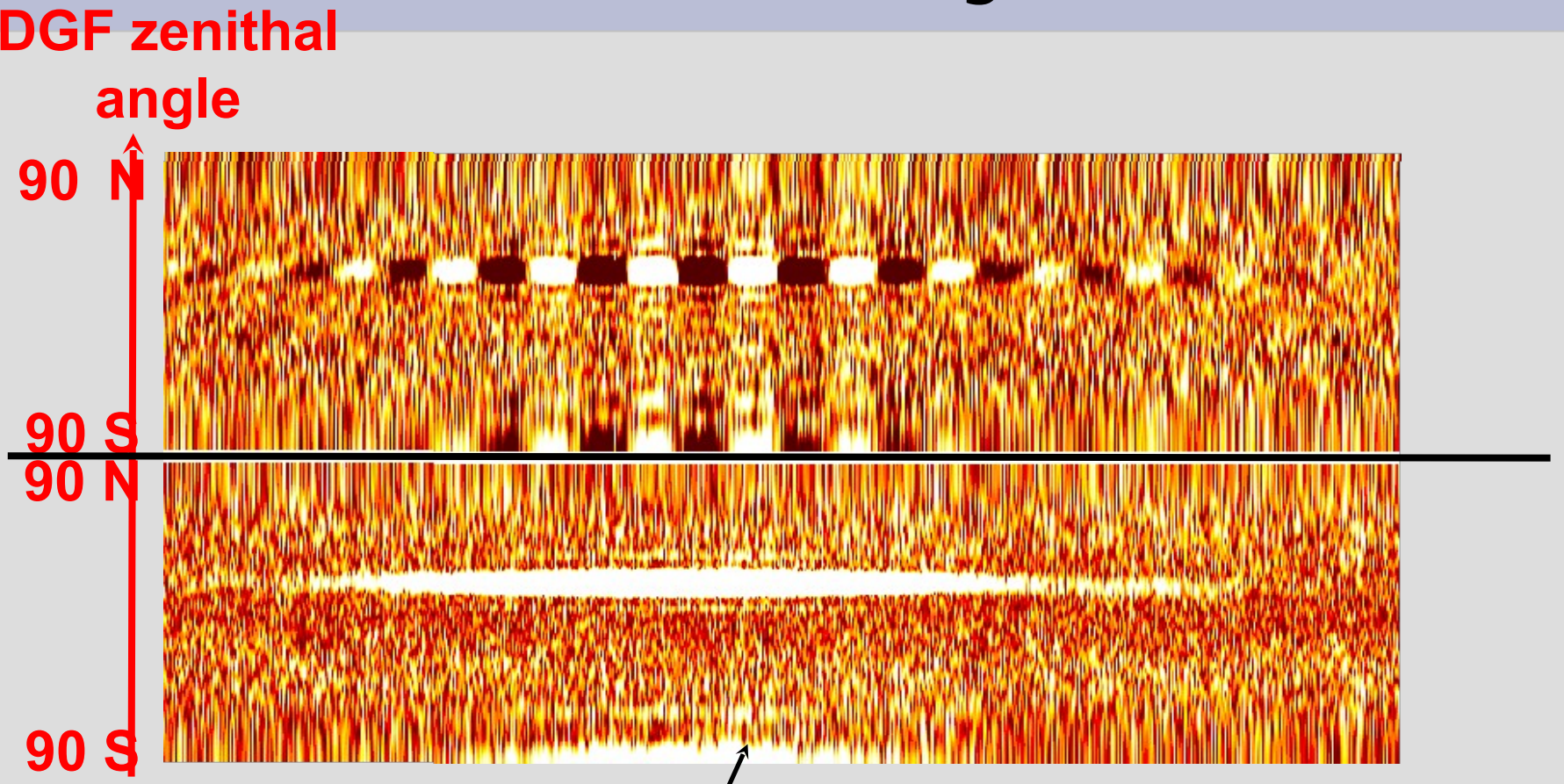
Nancay







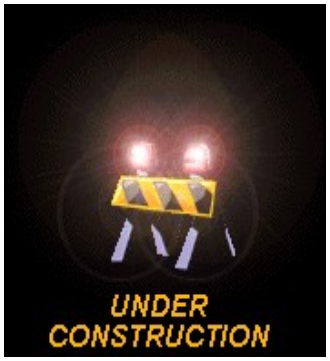
2D digital beam forming on CasA (<29 MHz>)
Nov 2009 Pittsburgh data



Analysis by C. Magneville / Irfu

En conclusion

- Powerful & versatile multi-channel acquisition system
  - Système distribué sur plusieurs centaine de m
  - Fréquence échantillonnage 500MHz sur une bande d'analyse de 1,5Gz
  - Taux de transfert de 500MB/s par voie électronique
  - Résolution temporelle entre voie ~10ps
  - 300MB/s pour traitement des données et écriture sur 1 PC
- En cours
  - Synchronisation multiprocesseurs
  - Corrélateur à base de FPGA


UNDER
CONSTRUCTION

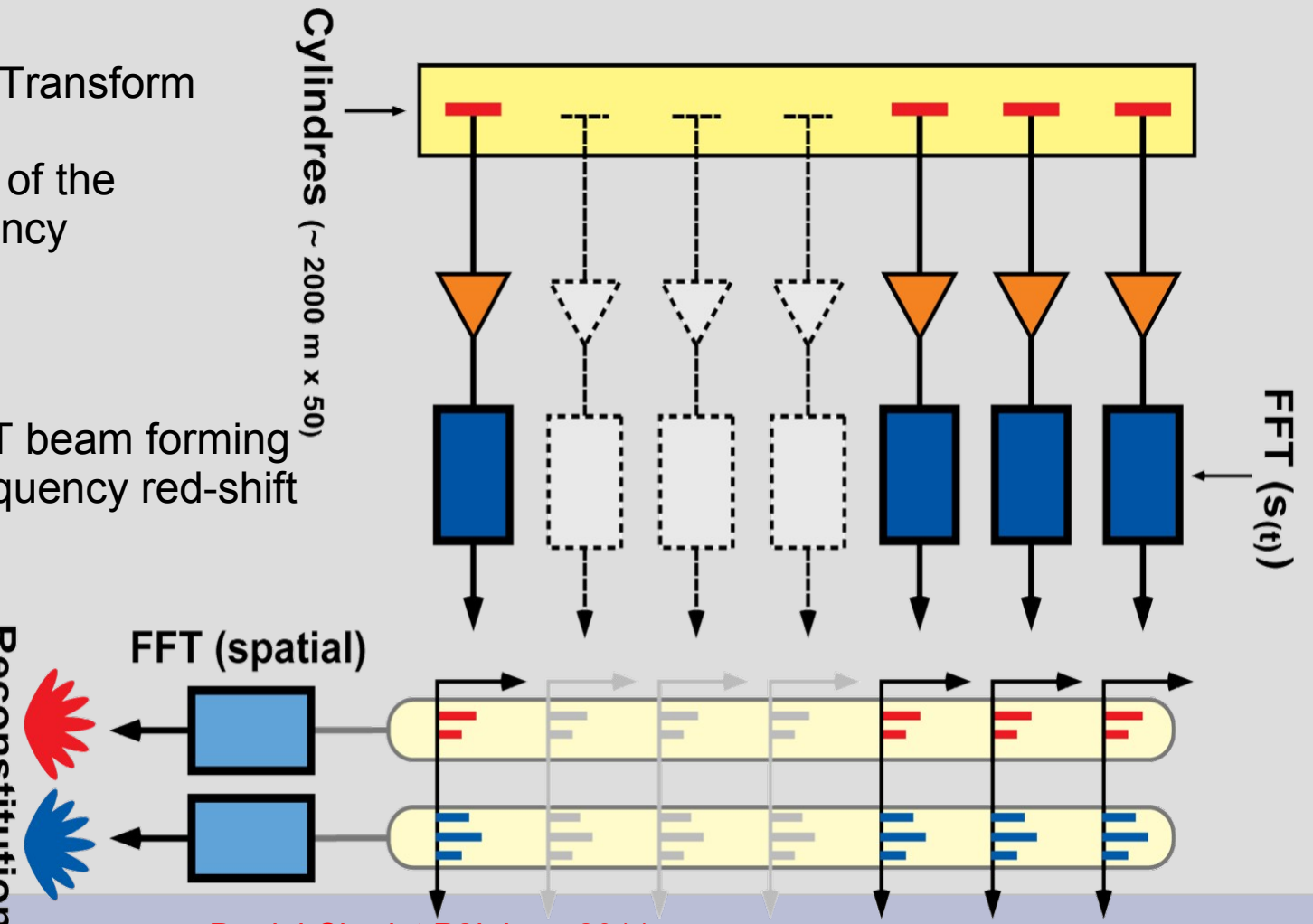
Numerical correlator

- Each channel:
  - Fast Fourier Transform
- ALL channel:
  - Combination of the
  - Same frequency

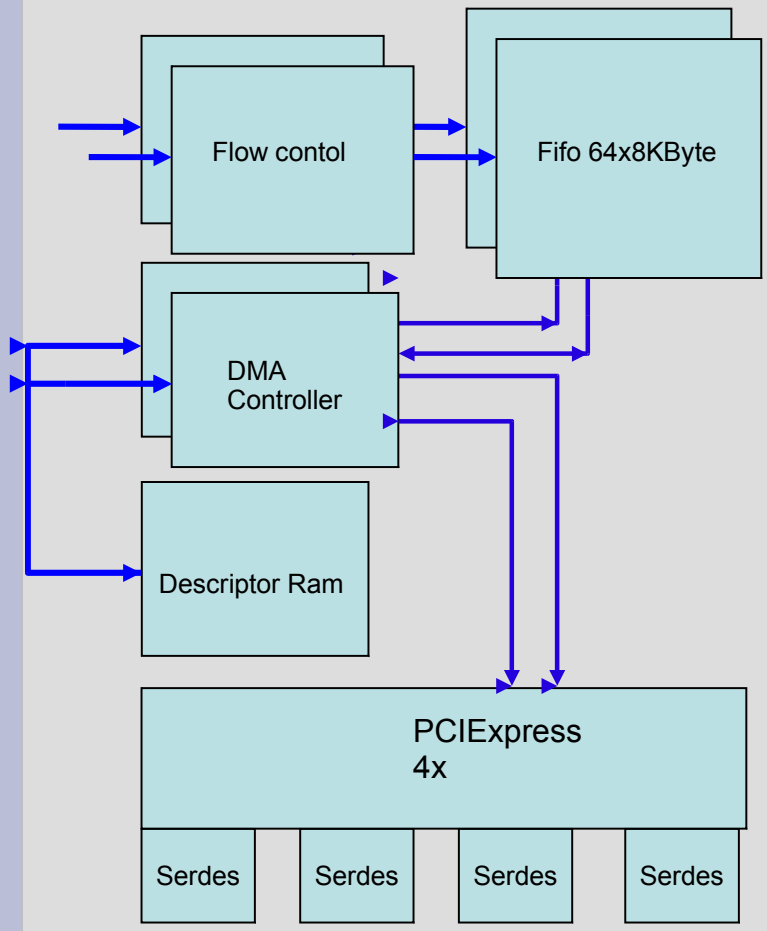
3 dimensions:

2 angles : FFT beam forming

Distance : frequency red-shift

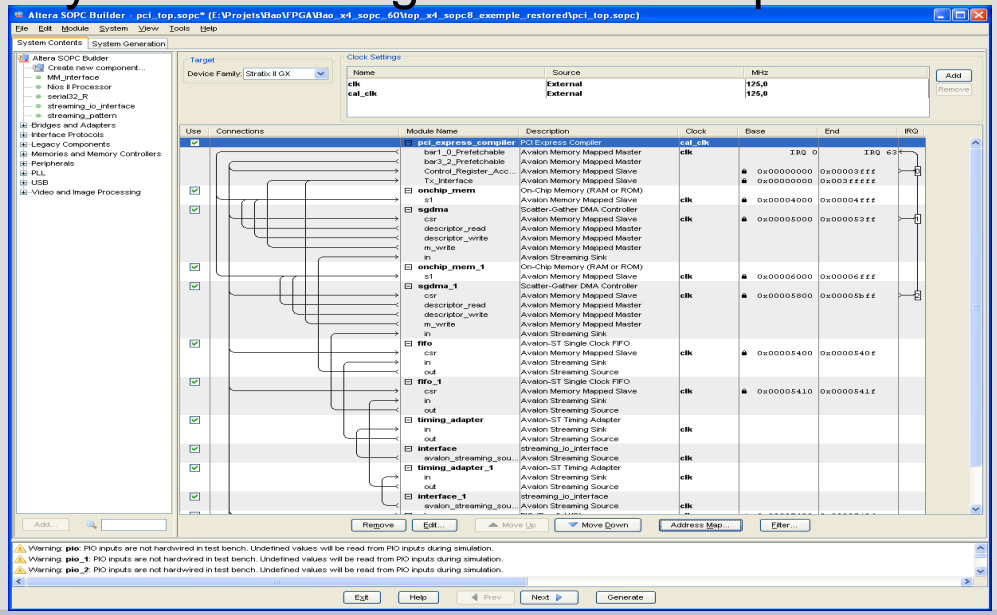


FPGA synoptic: PCIExpress interface



- FIFO buffering
- Scatter-gather DMA
- PCIExpress:
  - End point
  - 4X

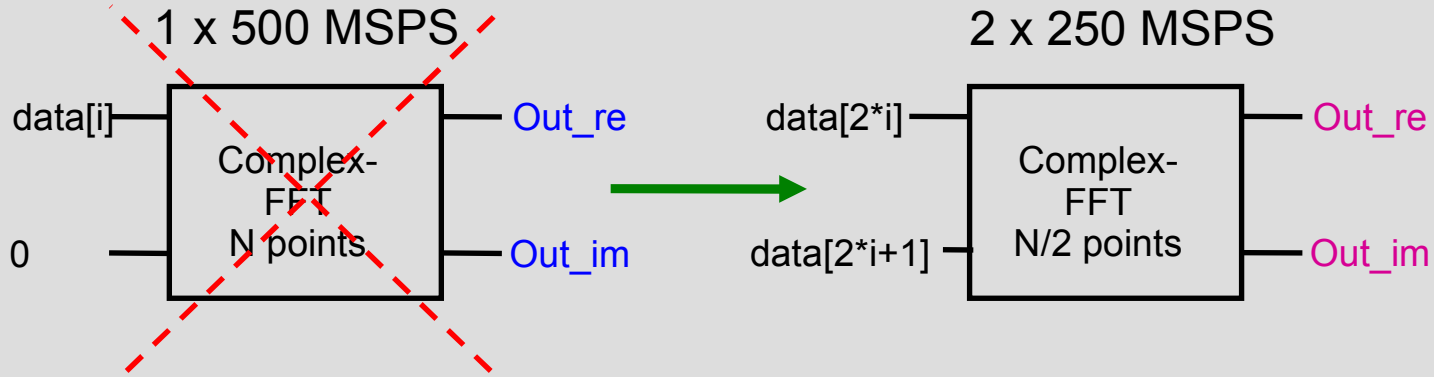
System On Programmable Chip module



Post ADC processing: Temporal FFT

FPGA Implementation of real-FFT using a IP Core:

to save hardware resources, we use a N/2 points complex-FFT to compute a N-points real-FFT



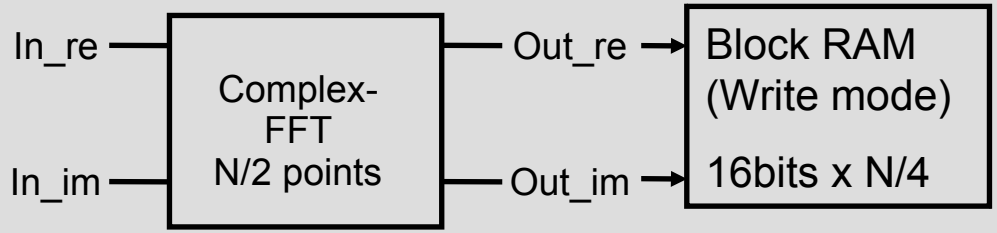
the real signal s[i=0:N-1] is transformed into a complex signal : c[i] = s[2*i] +j*s[2*i+1]

Post ADC processing: Temporal real-FFT

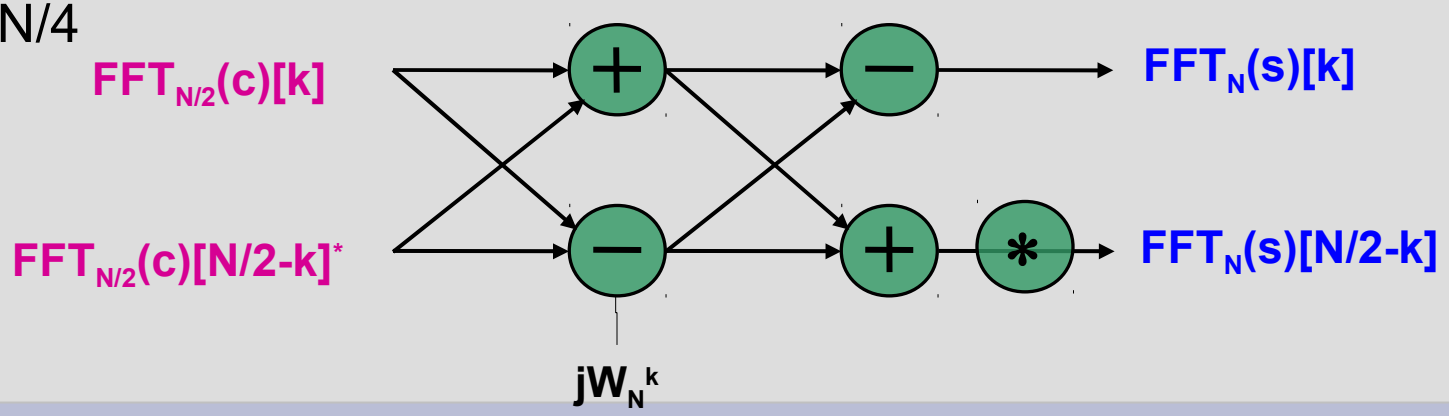
2 step computation:

- First step: N/4 clock cycles, we feed the block RAM with $FFT_{N/2}(c)[k]$

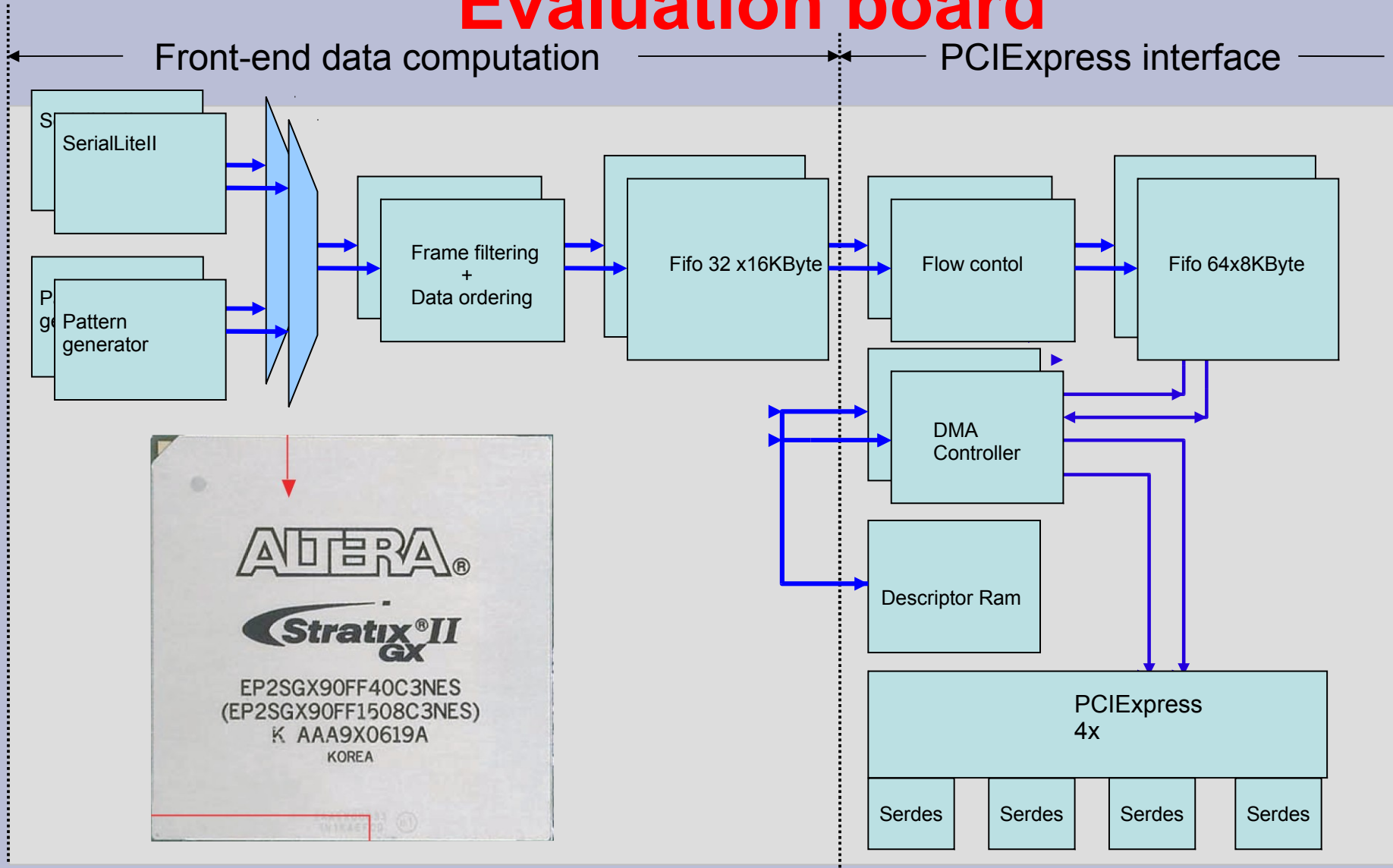
ADC output:
16 bits@250MHz
(2 time samples)



- Second step: N/4+1 clock cycles, the output of complex-FFT and data stored in block RAM feed 2 butterfly operators, for $0 \leq k \leq N/4$



Synoptic FPGA PCIExpress Evaluation board



ADC board FPGA Synoptic