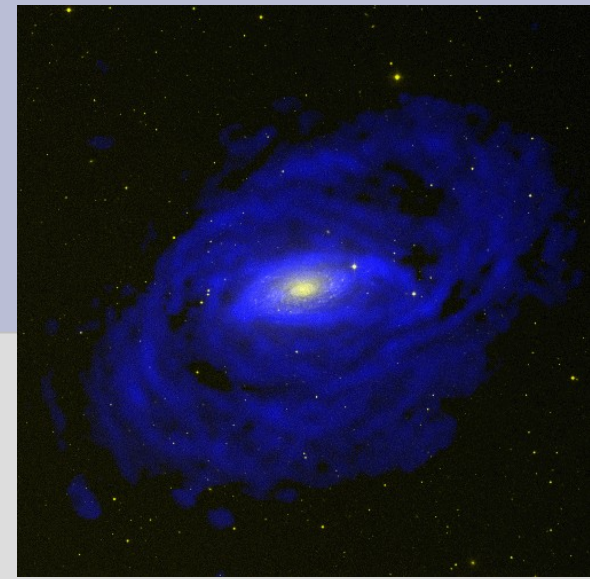




BAO radio

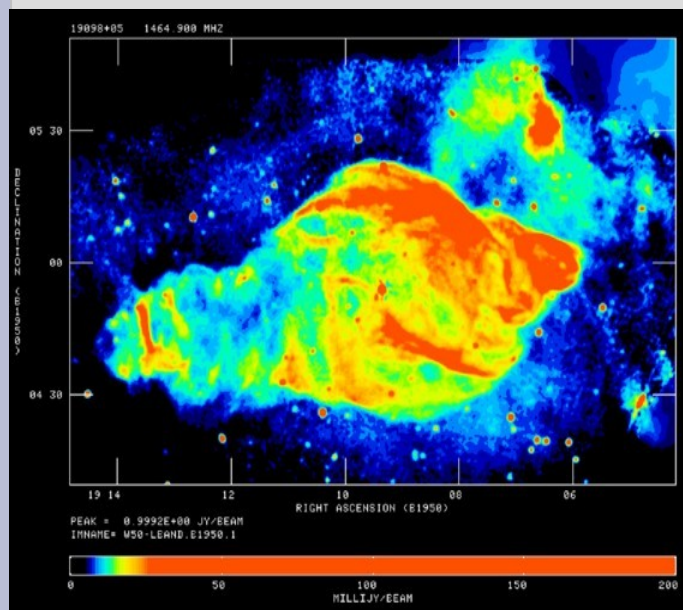
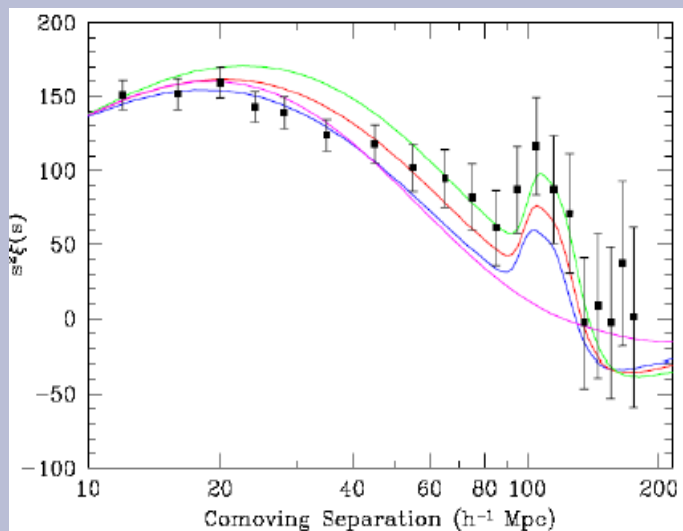


Systeme d'acquisition rapide pour un radio télescope multiple-voies

CEA/Irfu IN2P3/LAL CMU Fermilab colaboration



BAO : Baryonic Acoustic Oscillations



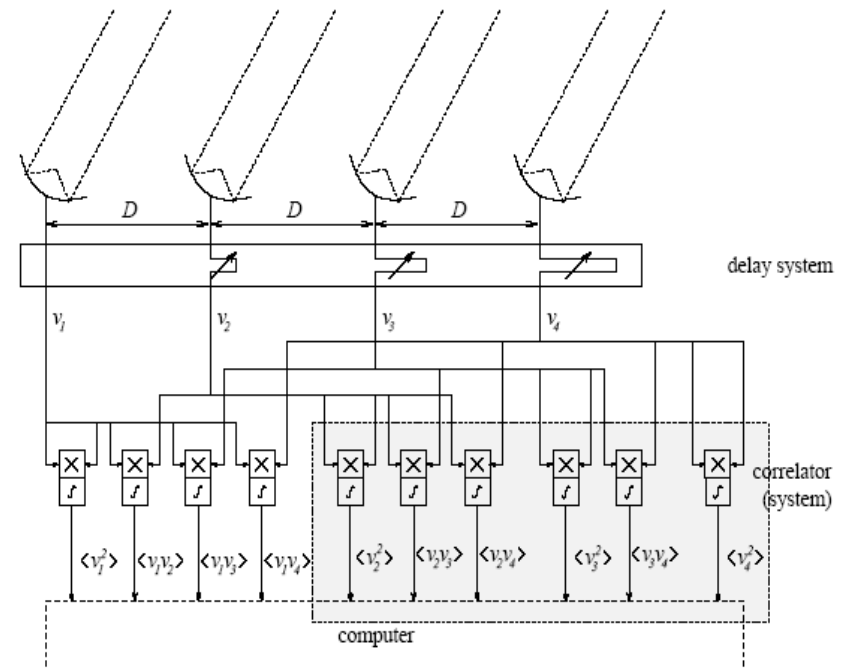
- Imprints left by the baryon-photon fluid (before recombination) in the distribution of ordinary (baryonic) matter
- Slight modulation of the distribution of matter, (and galaxies as tracers). Structure formation being mainly driven by CDM which dominates structure formation
- In Radio : Use 21 cm HI emission
- 3D HI mass distribution measurement through total 21 cm emission intensity mapping (No individual galaxy detection)
- Hyperfine transition (spin-orbit) of atomic hydrogen: $\nu \approx 1,420,405$ GHz $\rightarrow \lambda \approx 21$ cm



Concept: Interféromètre numérique

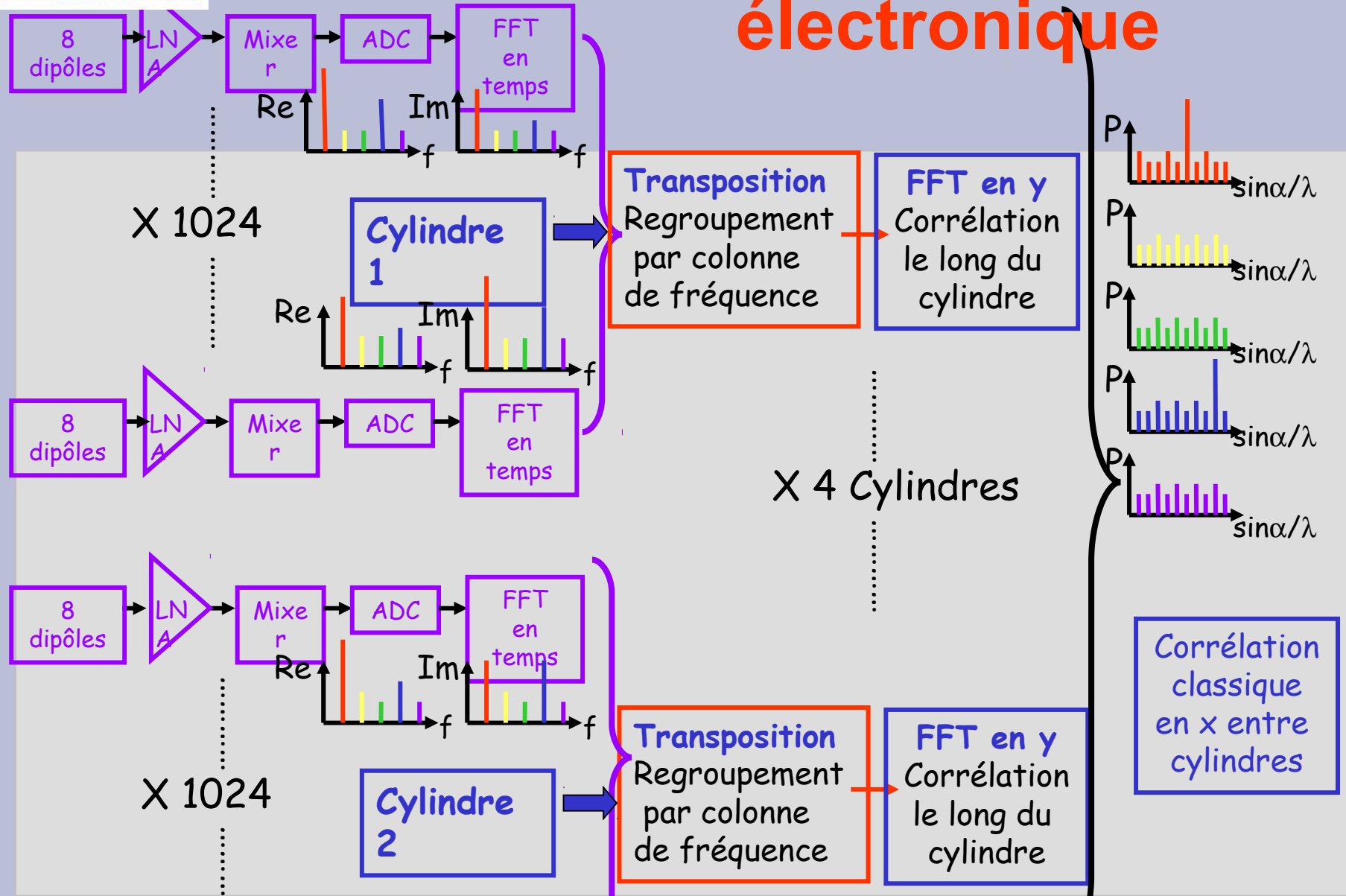
- Large field of view ($10\text{-}100 \text{ deg}^2$)
- ≥ 1000 simultaneous lobes \rightarrow Digital interferometer
- Wide band receivers 250 MHz
- Digital interferometer (correlator / beam-former)
- Resolution 10 arcmin, Surface $\geq 10\,000 \text{ m}^2$
- Reflectors over an area of $\sim 1000\text{-}2000 \text{ m} \times 1000\text{-}2000 \text{ m}$
- Cylindrical Radio Telescope concept or dish
- 256-512 electronic channel
- 4 bands of 250MHz between 0.5-1.5GHz
- Sampling at 500MHz
- Possible implantation in China

Array and corrélation



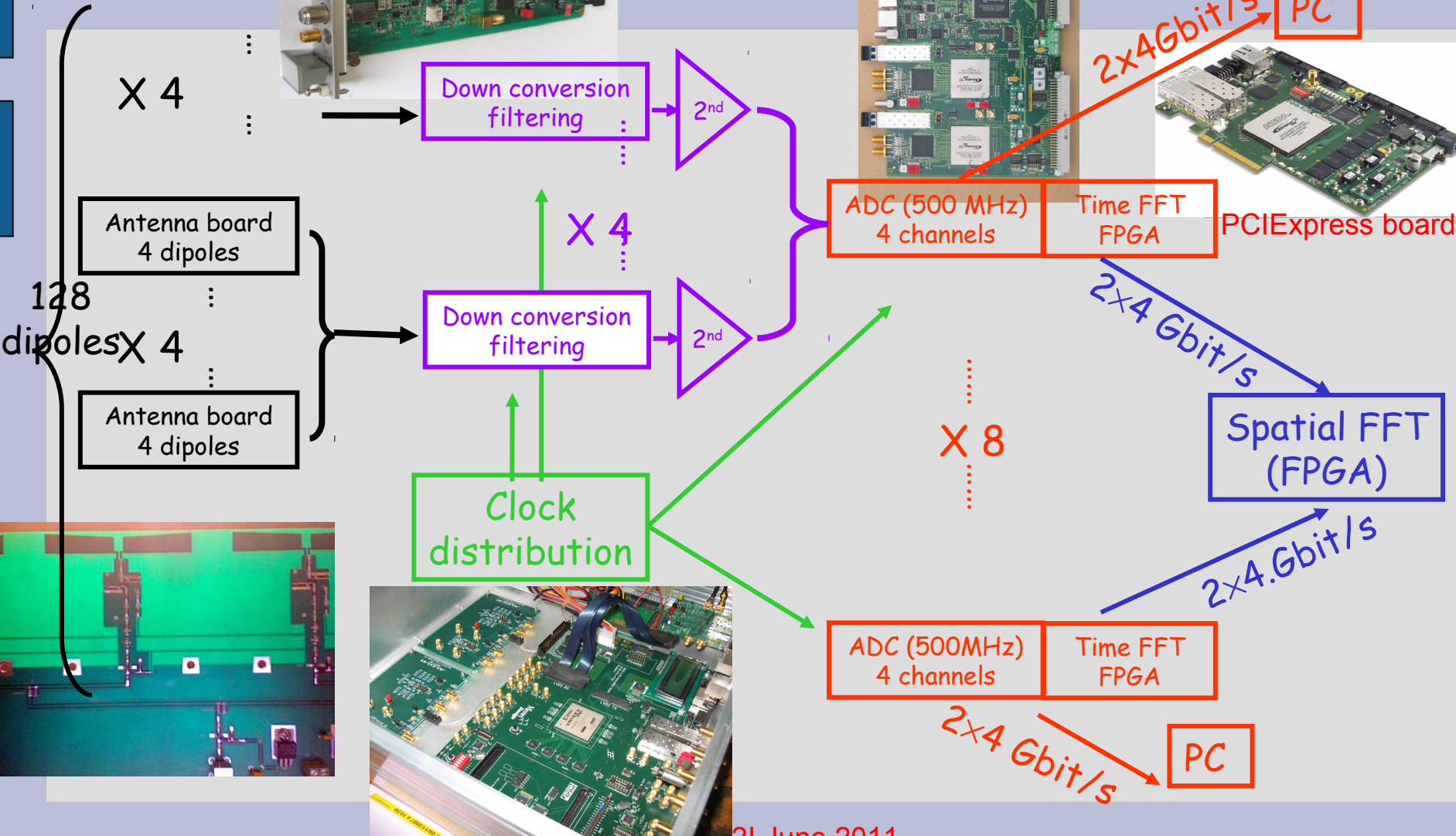
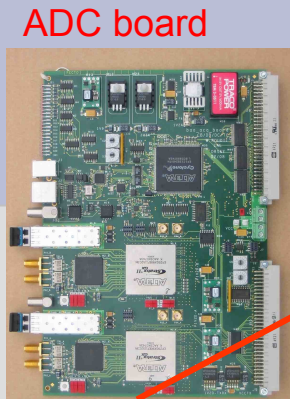


Schématique de la chaîne électronique





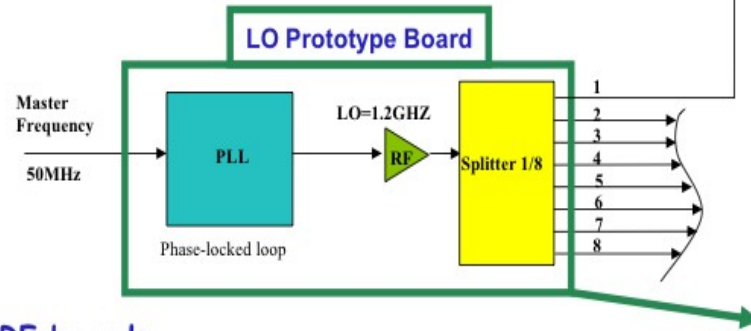
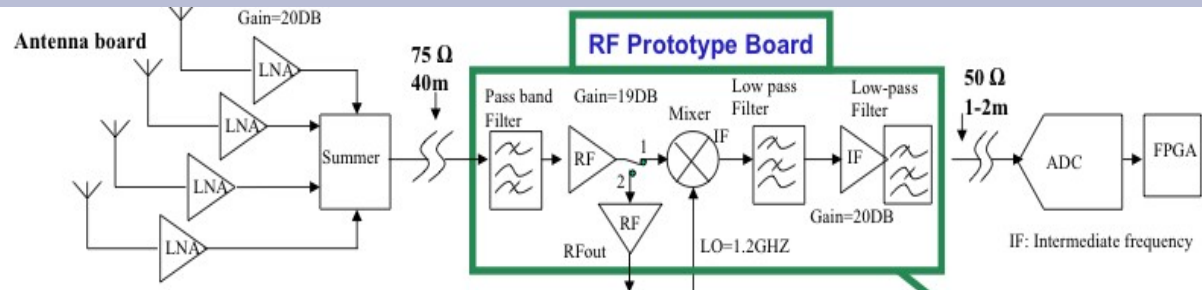
Chaîne électronique





Chaîne analogique prototype RF

CEA irfu



Local Oscillator → RF amplifier, mixer



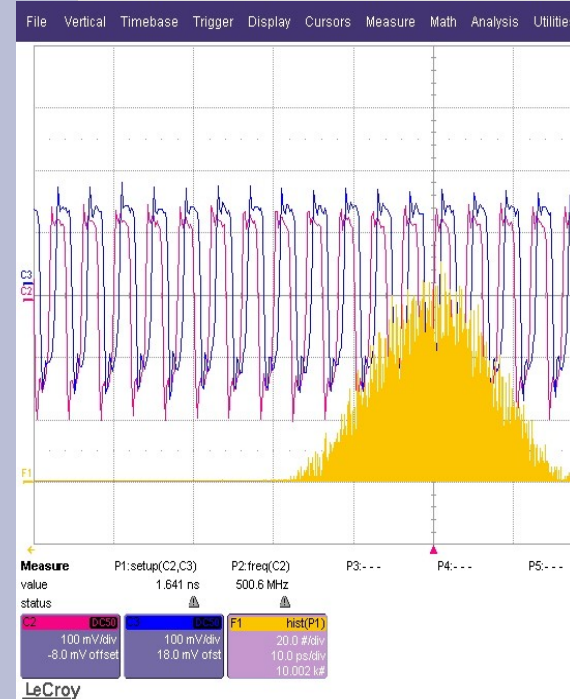
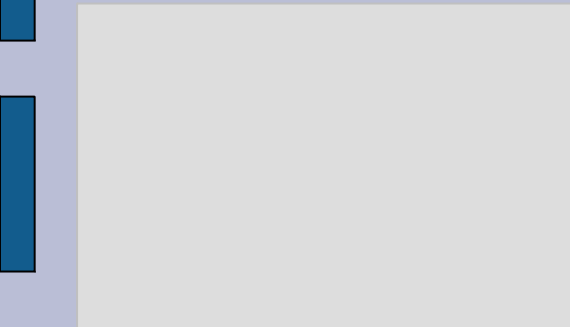
Front panel plug-in (3U EuroCard)

RF board:

- 75Ω/50Ω inputs
- 2 channels per board
- Possibility of by-passing mixer to test the under-sampling approach.
- Possibility to "tune" the pass band filter

BAO Radio HSHS project

January 10, 2008



Timebase	0.0 ns	Trigger	C2
	5.00 ns/div	Normal	8 mV
	500 S	10 GS/s	Edge
			Positive

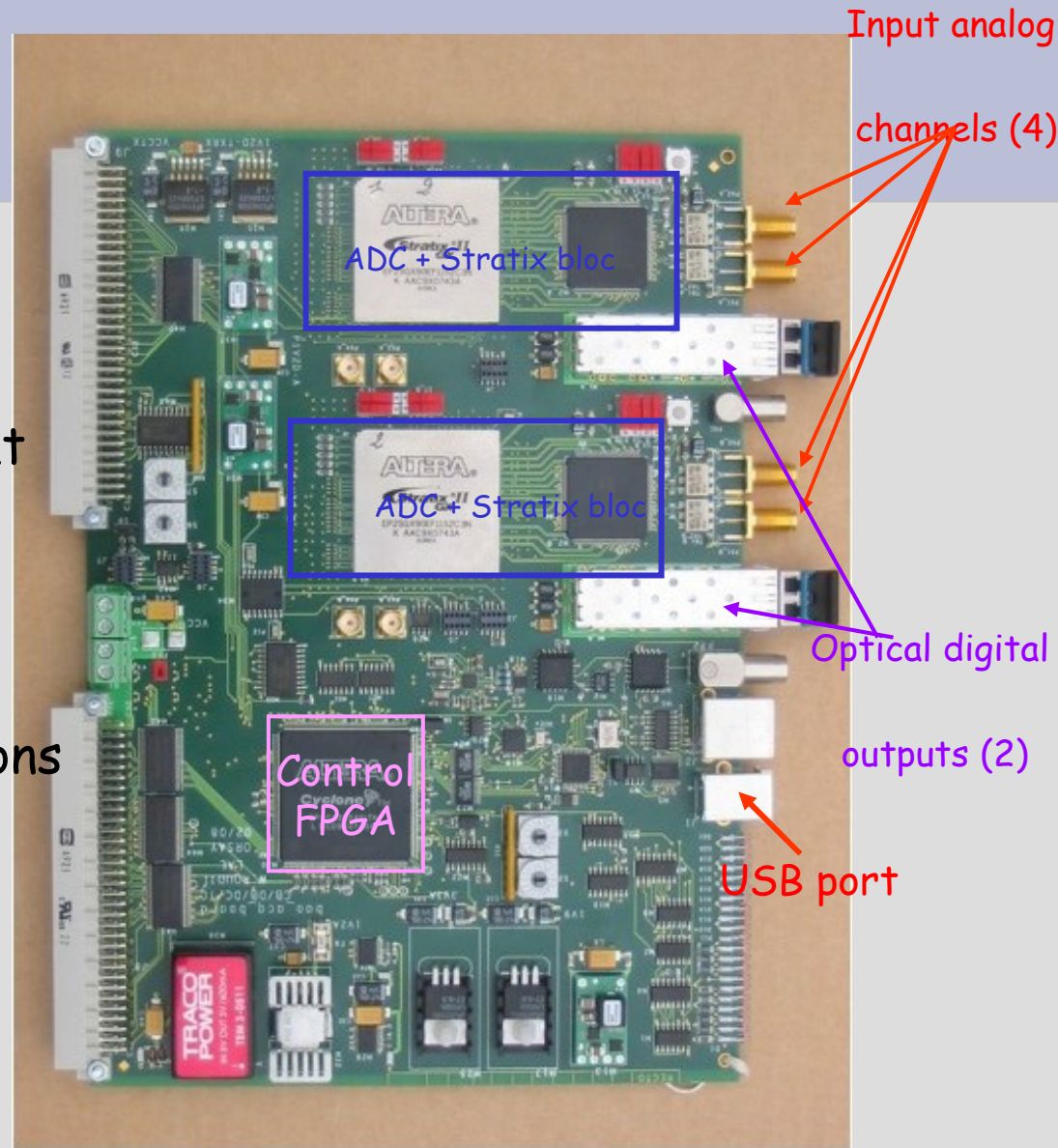
7/5/2007 1:45:16 PM



Carte ADC 500MHz

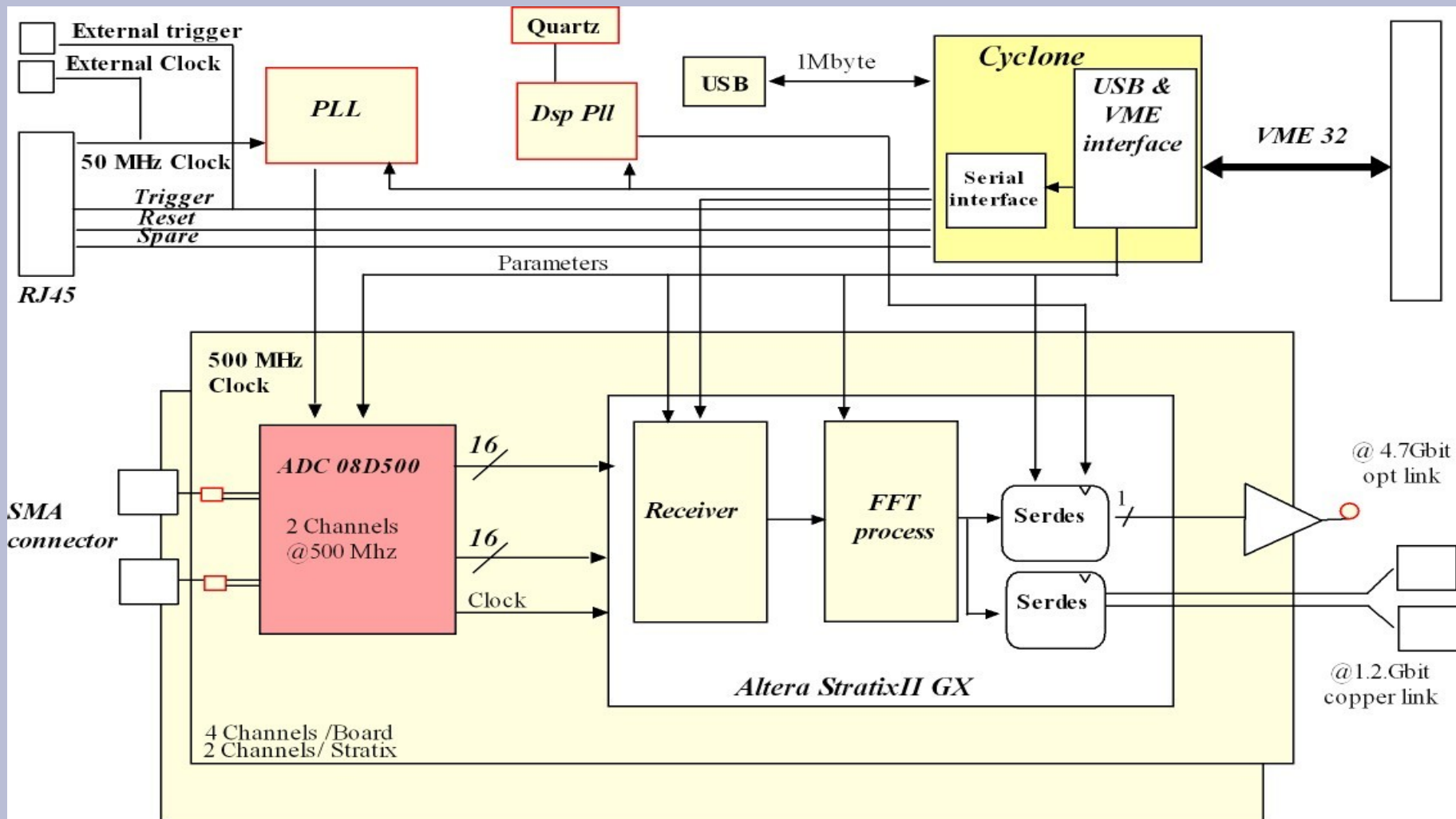
Each ADC board has :

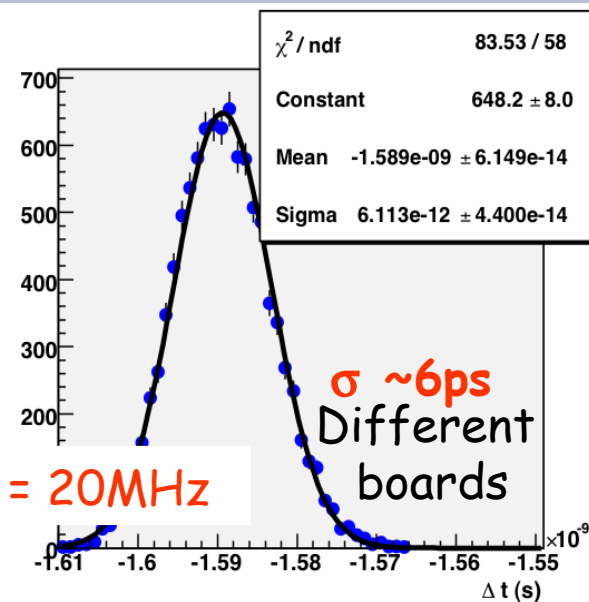
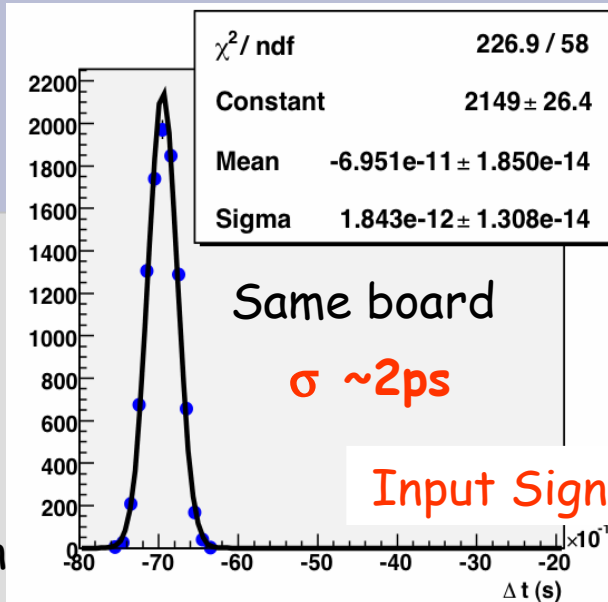
- 4 input channels (digitized at 500 MHz max)
- Input clock + control (start/stop...) ports
- USB, and VME communications port (for control)
- 2 high speed (4.8 Gbit/s) optical outputs (data links to PCI-express boards)





Synoptique carte ADC

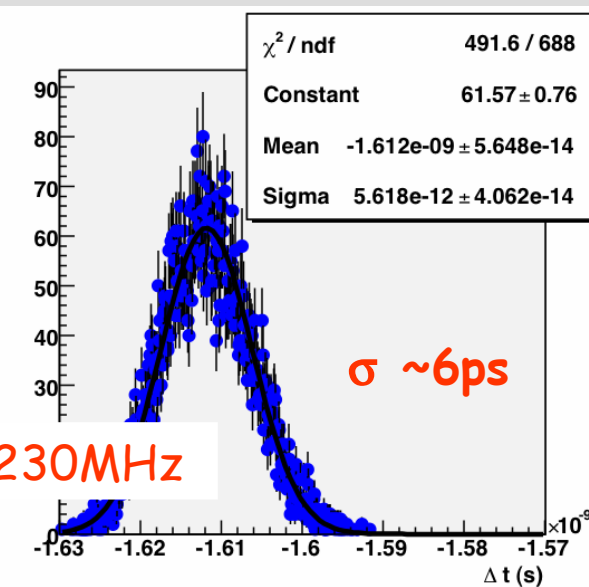
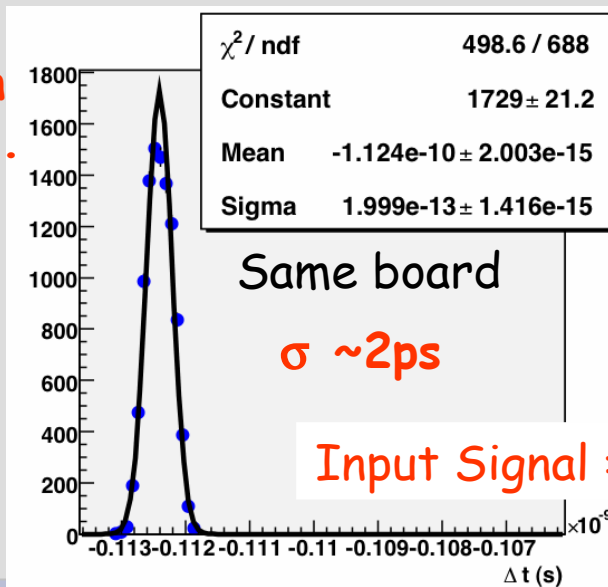




Input Signal = 20MHz

➤ Lot of work on pll used in ADC board to get a stable 500 MHz clock.

➤ Time resolution between channel better than 10 ps.

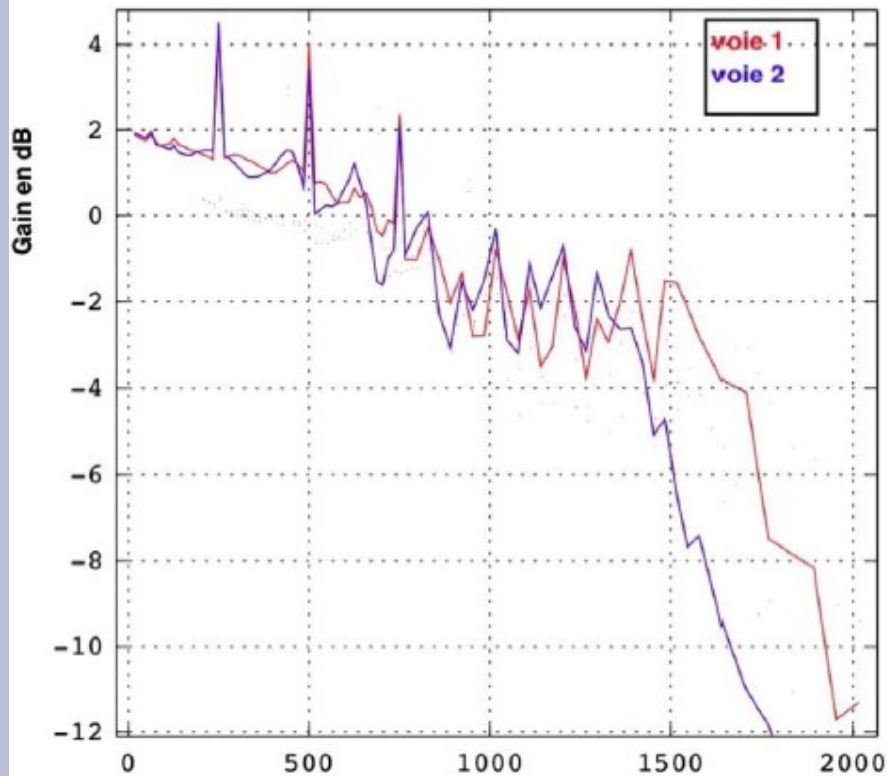


Input Signal = 230MHz

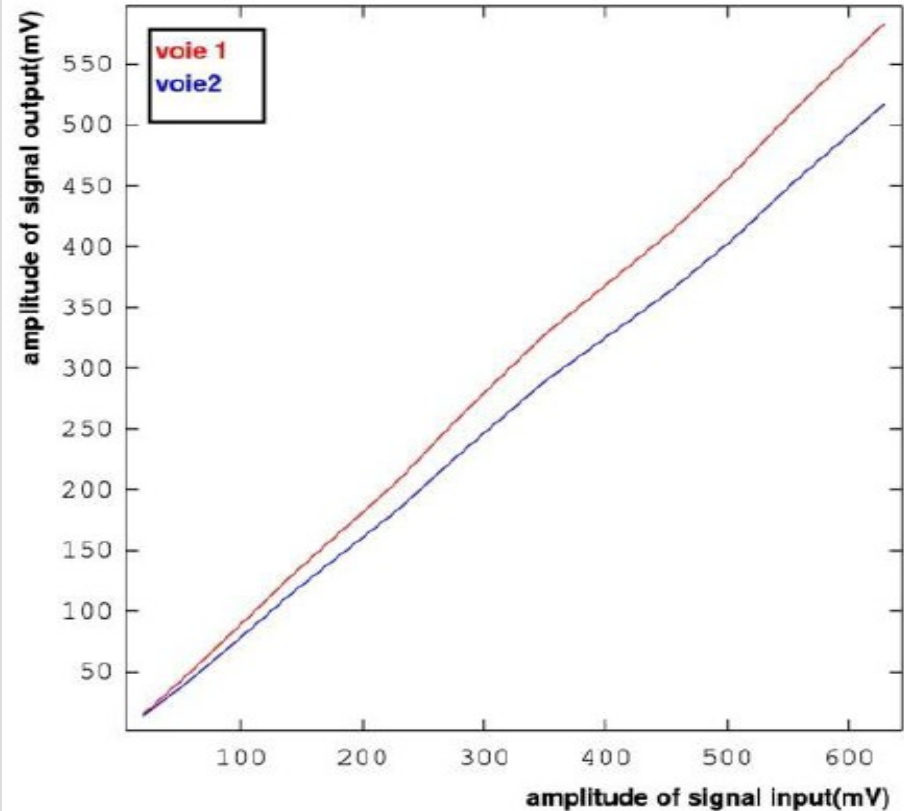


Caractéristique analogique

Bode diagram

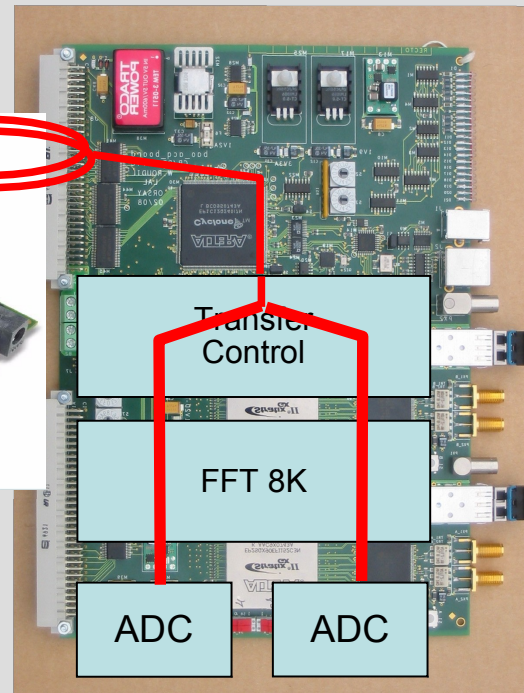
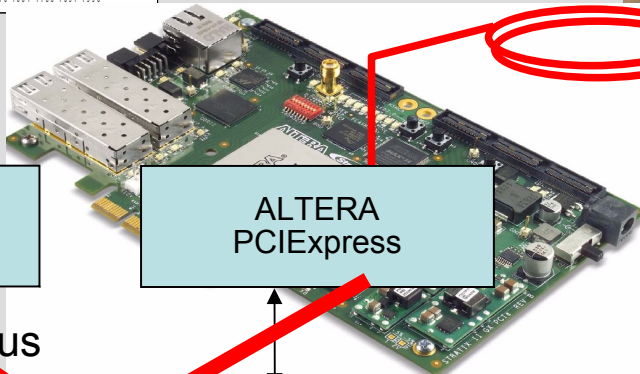
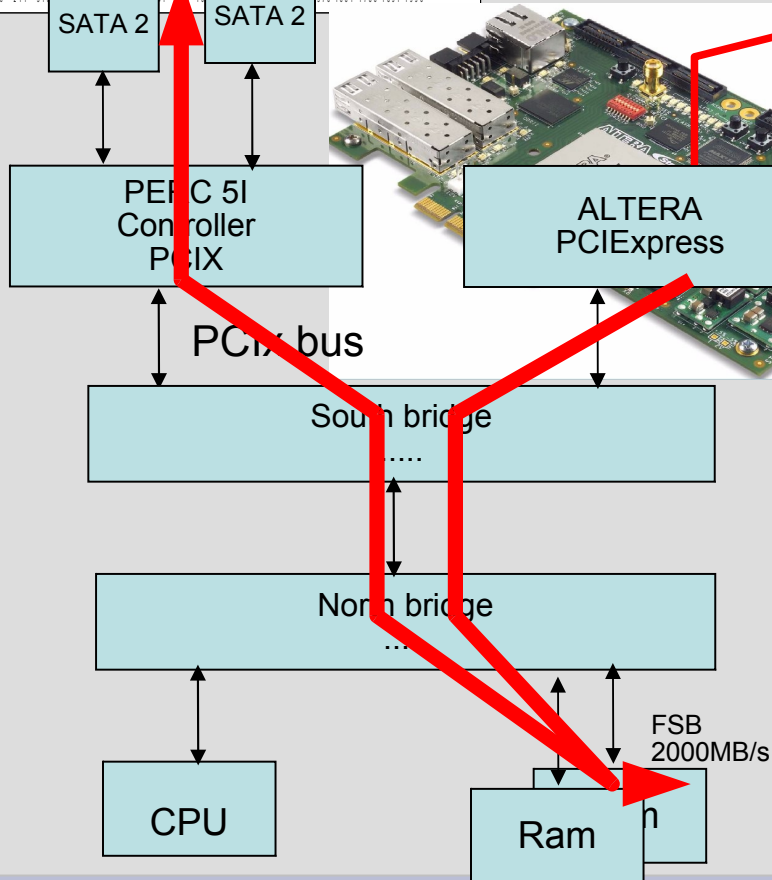
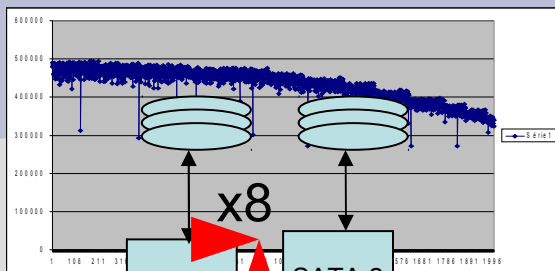


Linearity at 1.4GHz





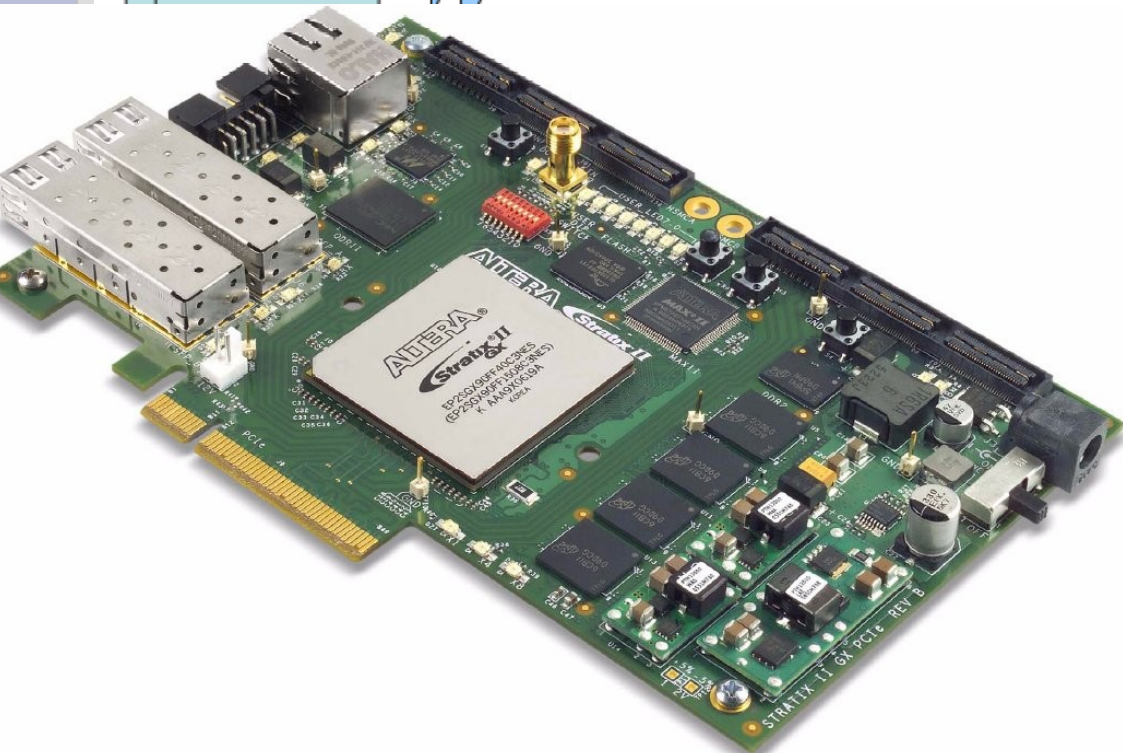
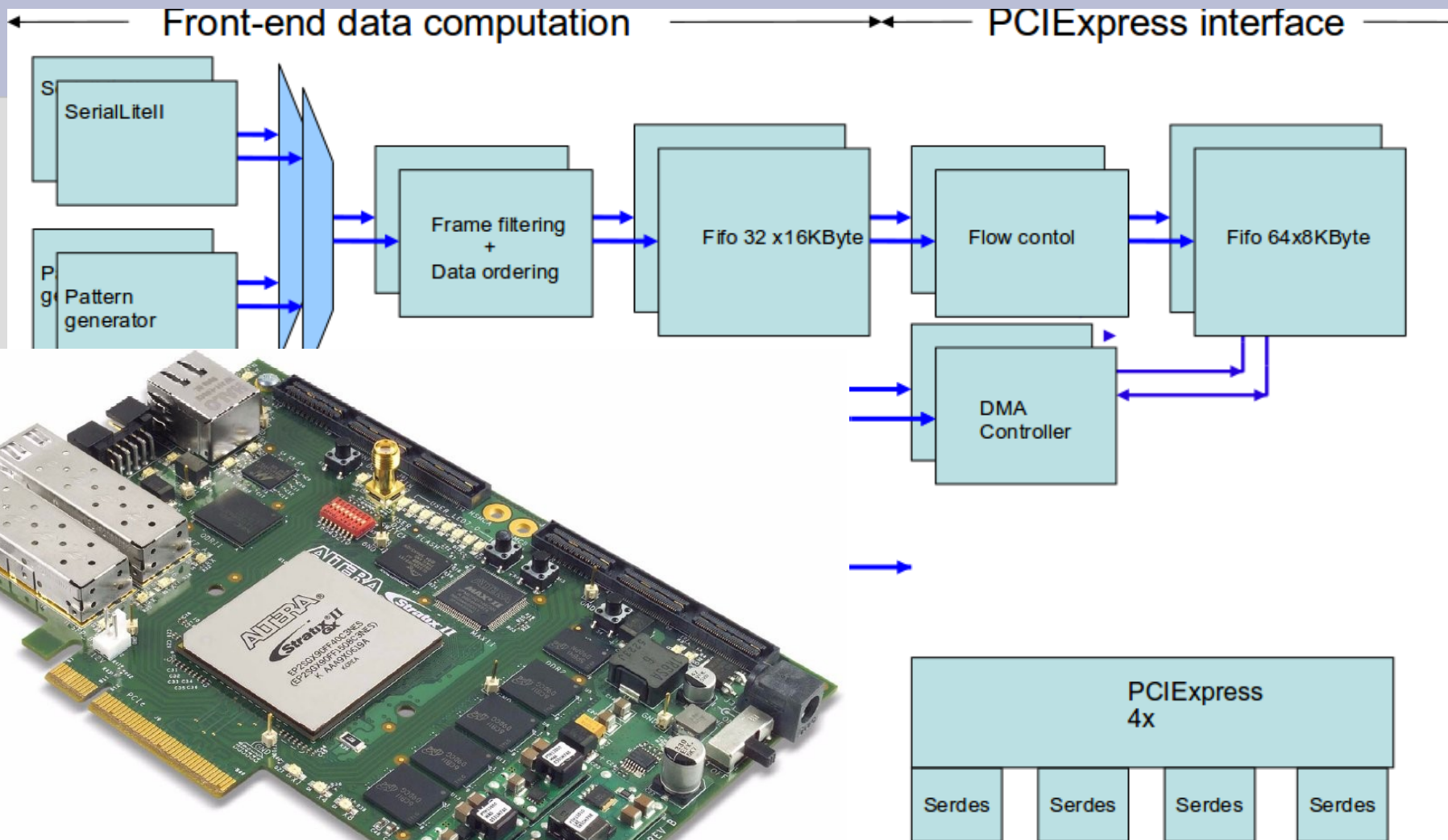
Test système acquisition



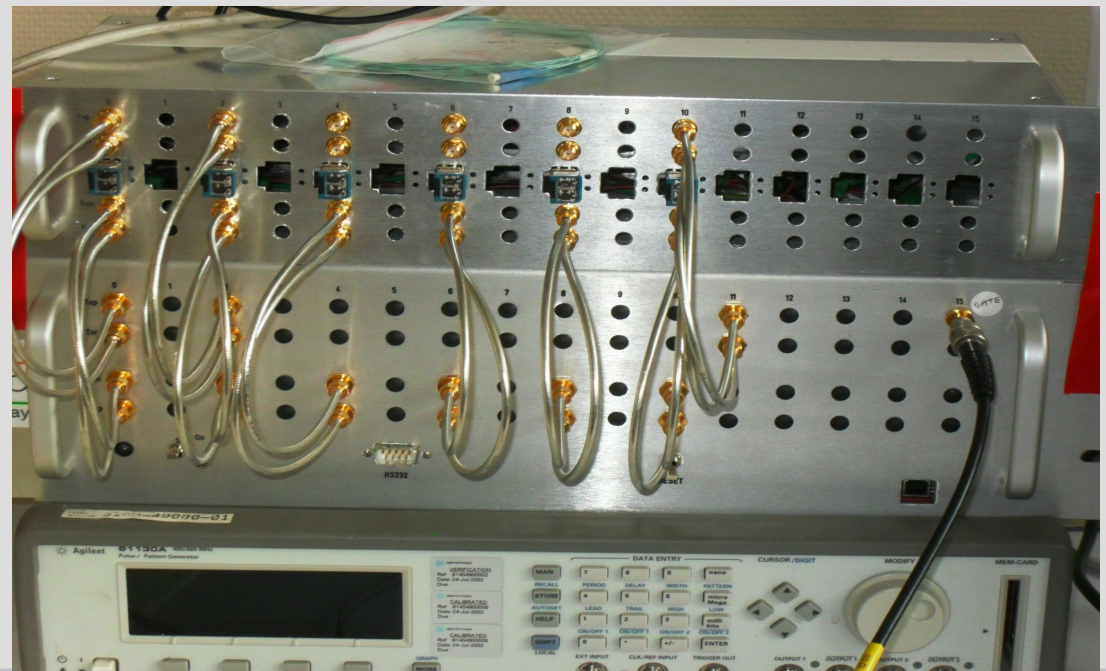
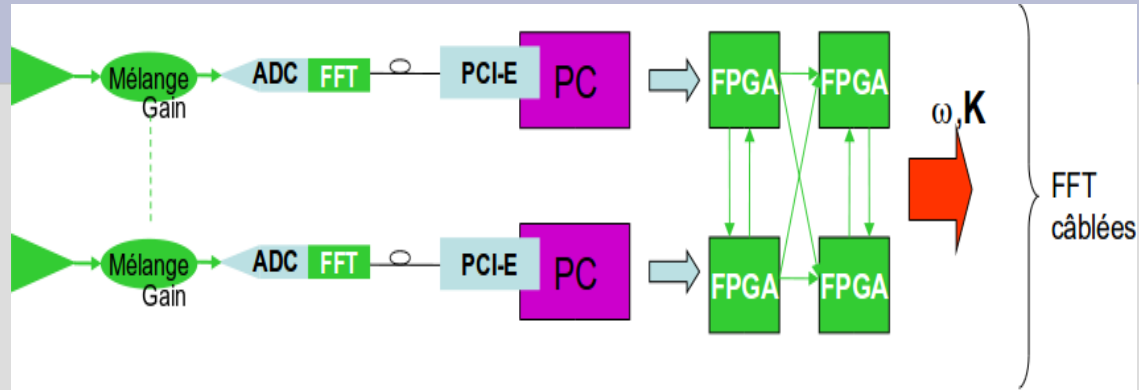
- DMA transfer
- Disk writing
- Cpu treatment
- Multi hardware tested
- Multi OS tested



PCIExpress: carte évaluation



Corrélateur





Transfert des données sur PC

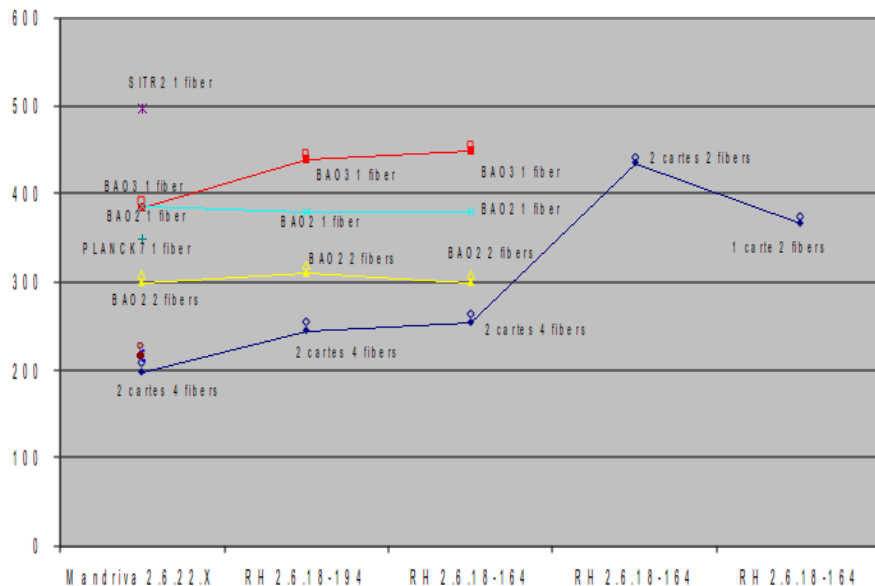
Multi-thread acquisition software:
PCIExpress DMA
Disk write

PCIExpress DMA transfert :

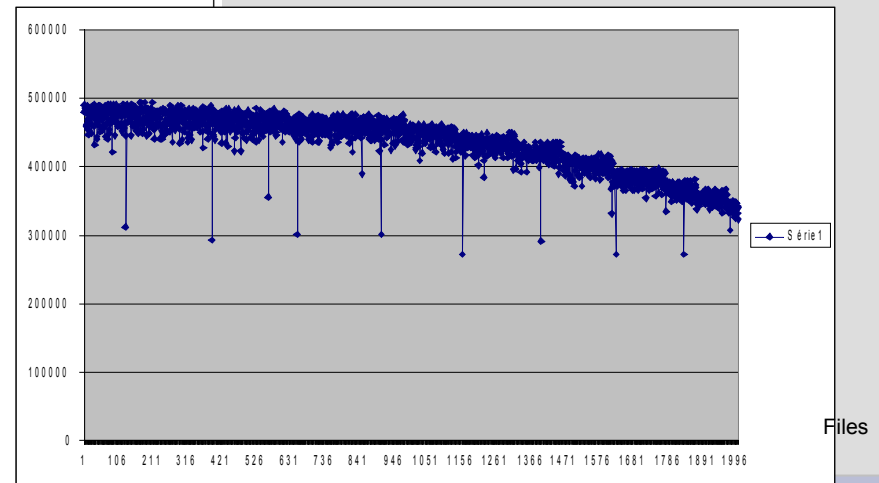
Average throughput 430MB/s

300MB/s substained data rate from
digitilizer to PC-disk

BAO3 : PowerEdge R710 BAO2 : PowerEdge T100
SITR2 NBPLANCK7 : Poweredge 2900

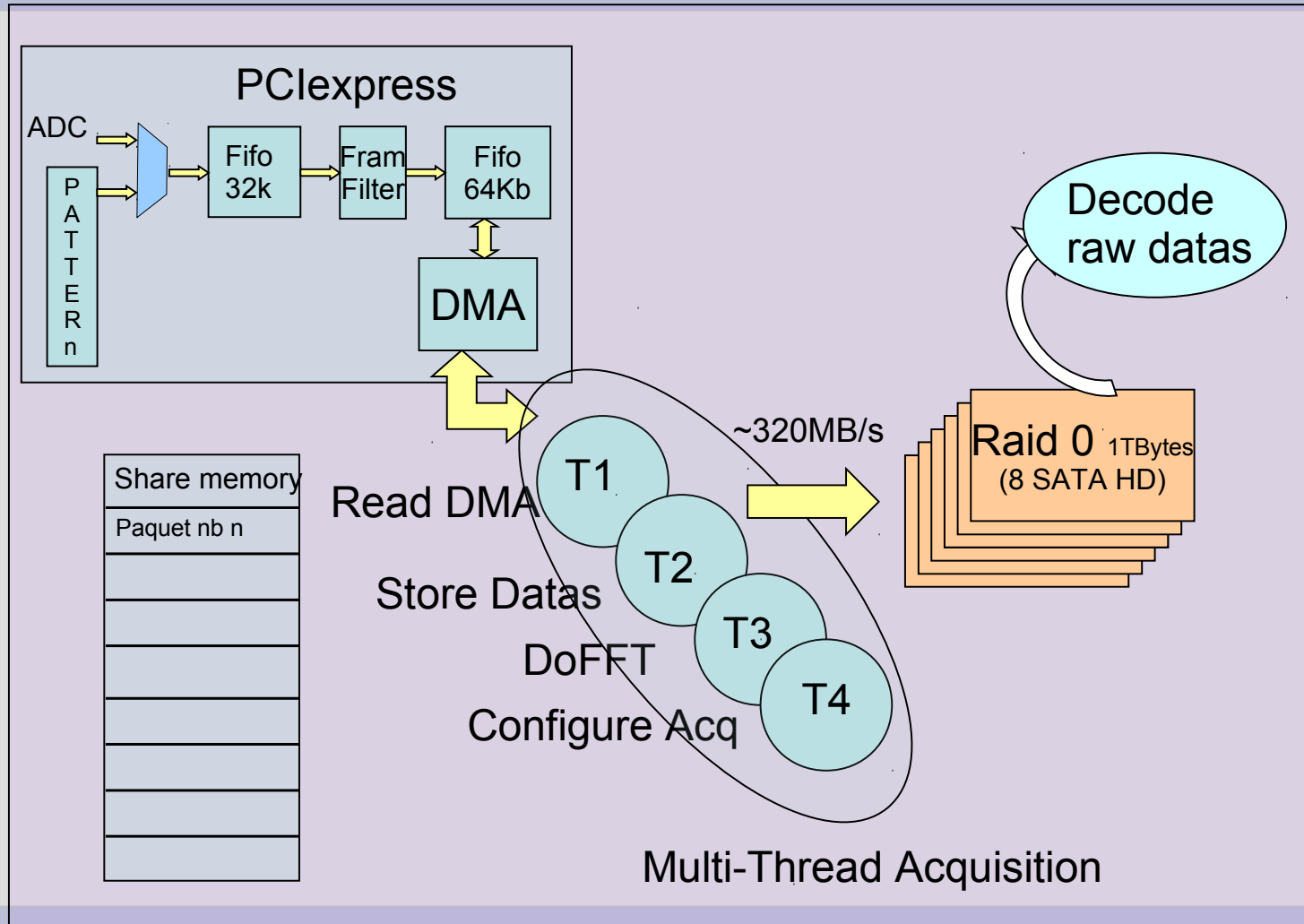


MByte/S



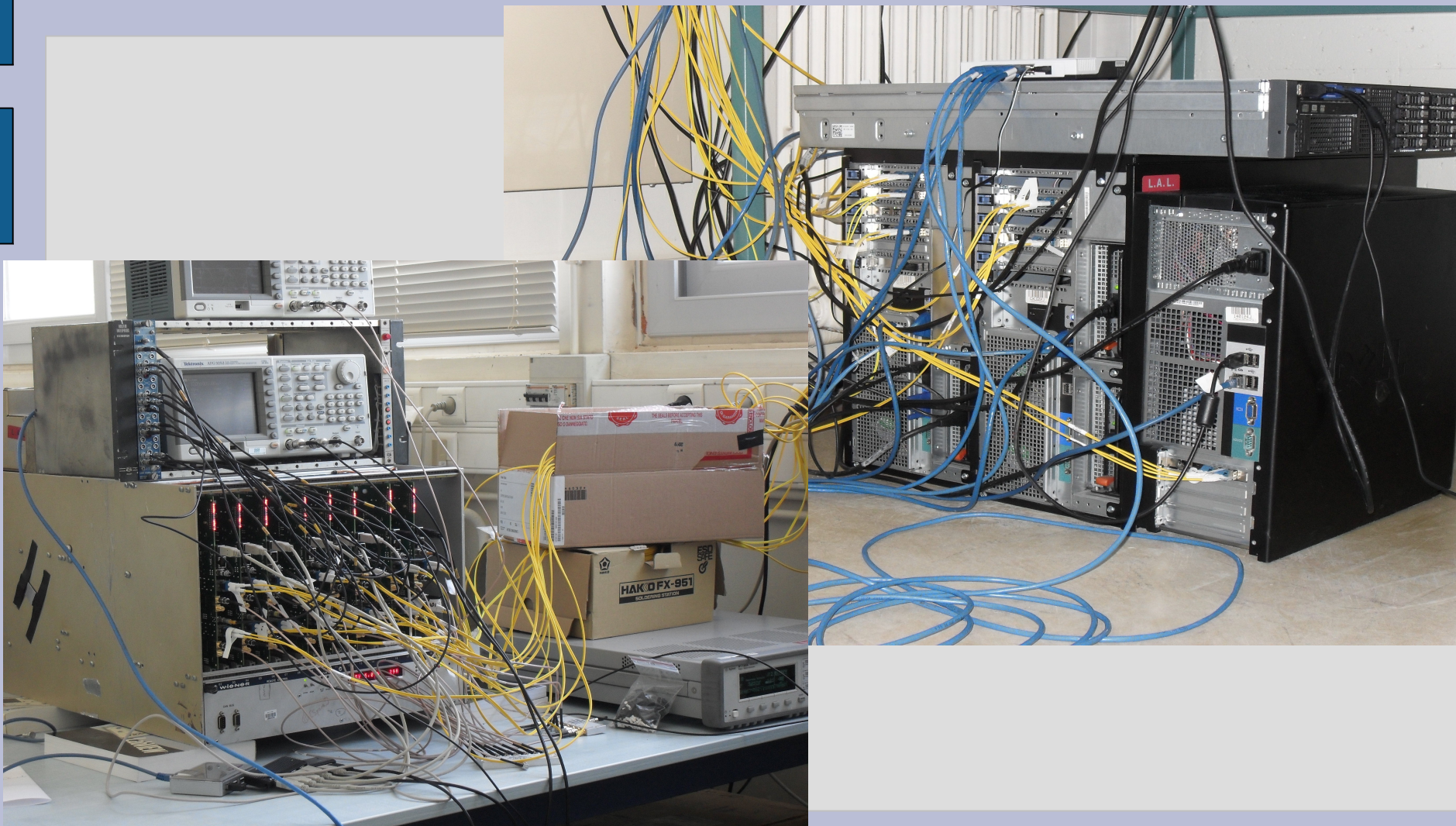


Acquisition des données





Systeme acquisition prototype





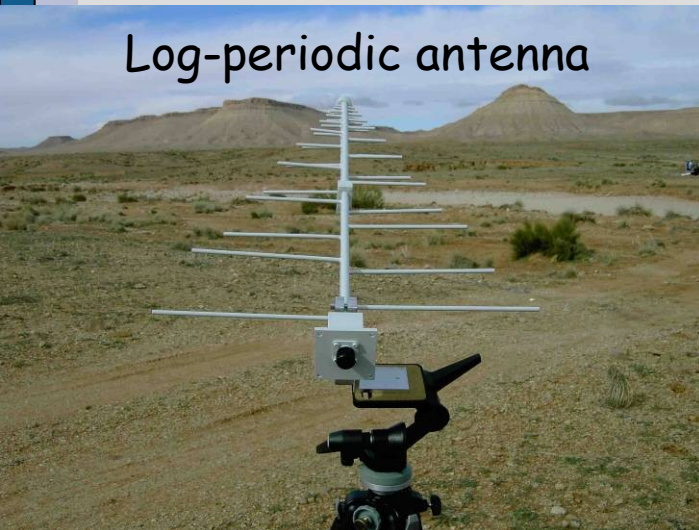
Systeme experimental

In Nançay (Juil 2008)

Before BAO_ADC board was ready,
acquisition was based on Matakq14 board



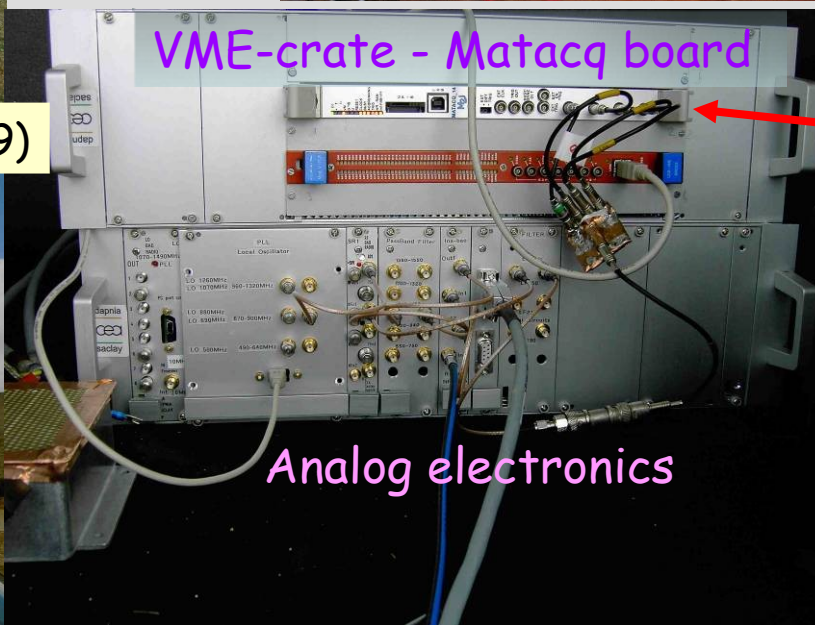
Log-periodic antenna



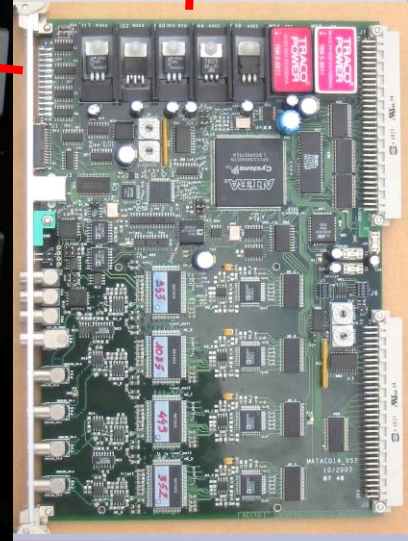
In the Morrocan desert (Jan 2009)



VME-crate - Matakq board



Analog electronics





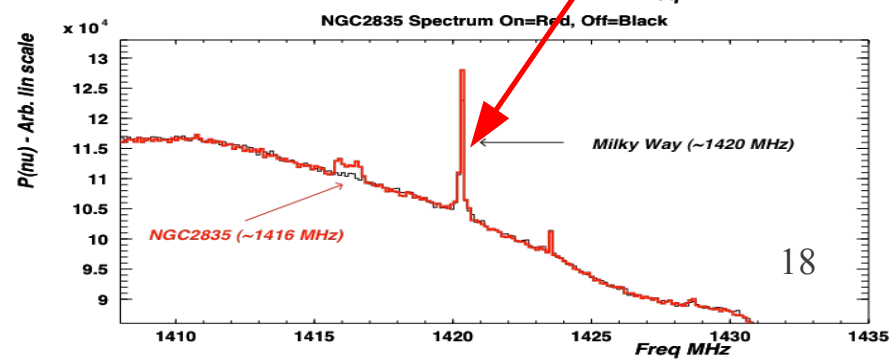
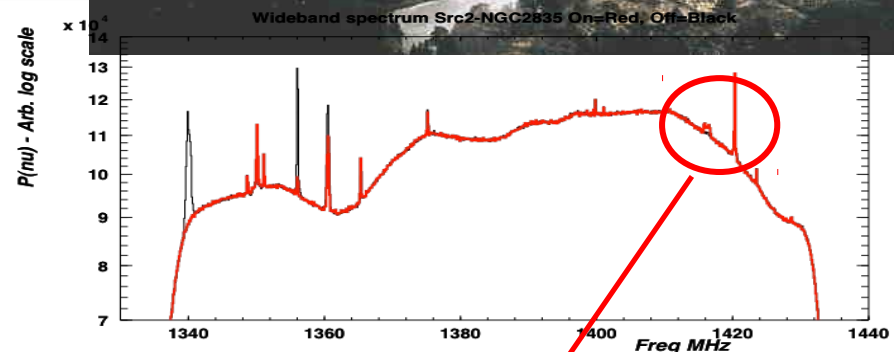
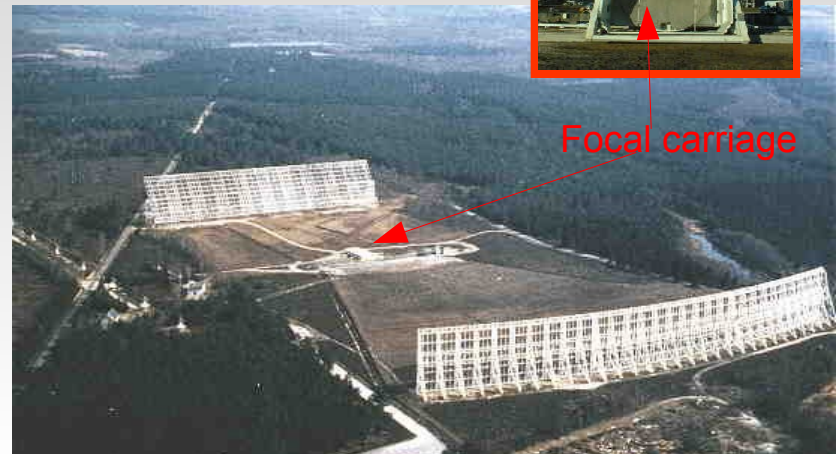
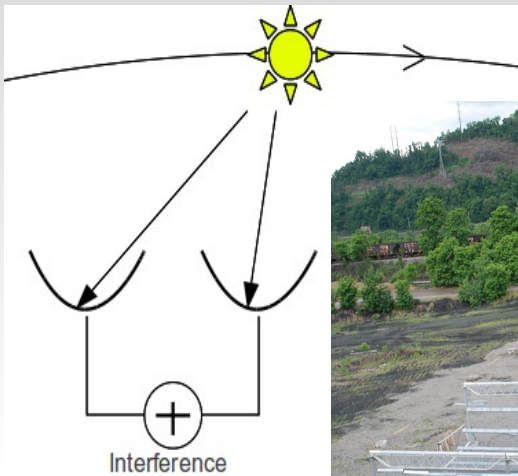
Test sur site

Pittsburgh

Nancay



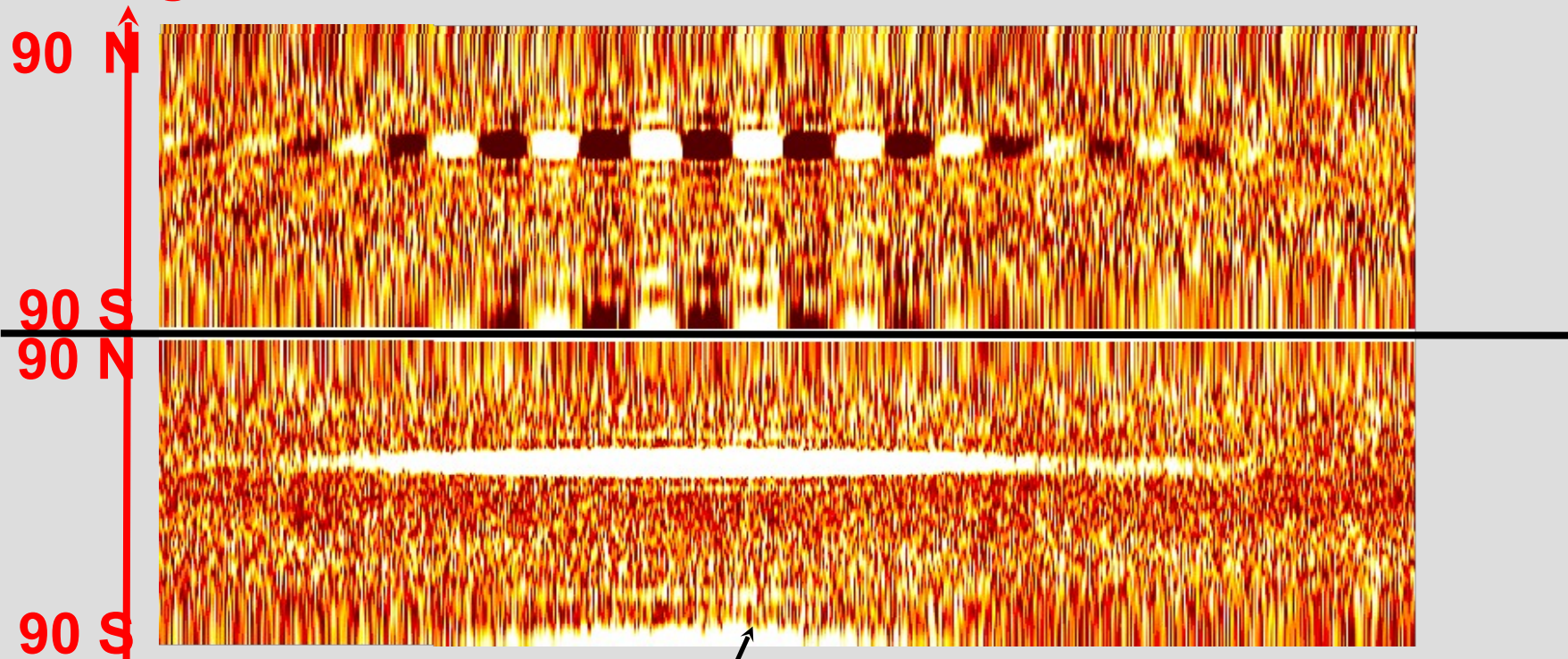
Focal carriage



2D digital beam forming on CasA (<29 MHz>)

Nov 2009 Pittsburgh data

DGF zenithal
angle



Analysis by C.
Magneville / Ifu

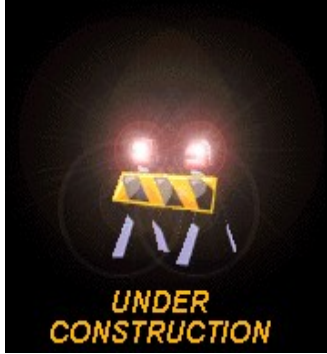
Grating first order diffraction

Time
(RA)



En conclusion

- Powerful & versatile multi-channel acquisition system
 - Système distribué sur plusieurs centaines de m
 - Fréquence échantillonnage 500MHz sur une bande d'analyse de 1,5Gz
 - Taux de transfert de 500MB/s par voie électronique
 - Résolution temporelle entre voie ~10ps
 - 300MB/s pour traitement des données et écriture sur 1 PC
- En cours
 - Synchronisation multiprocesseurs
 - Corrélateur à base de FPGA





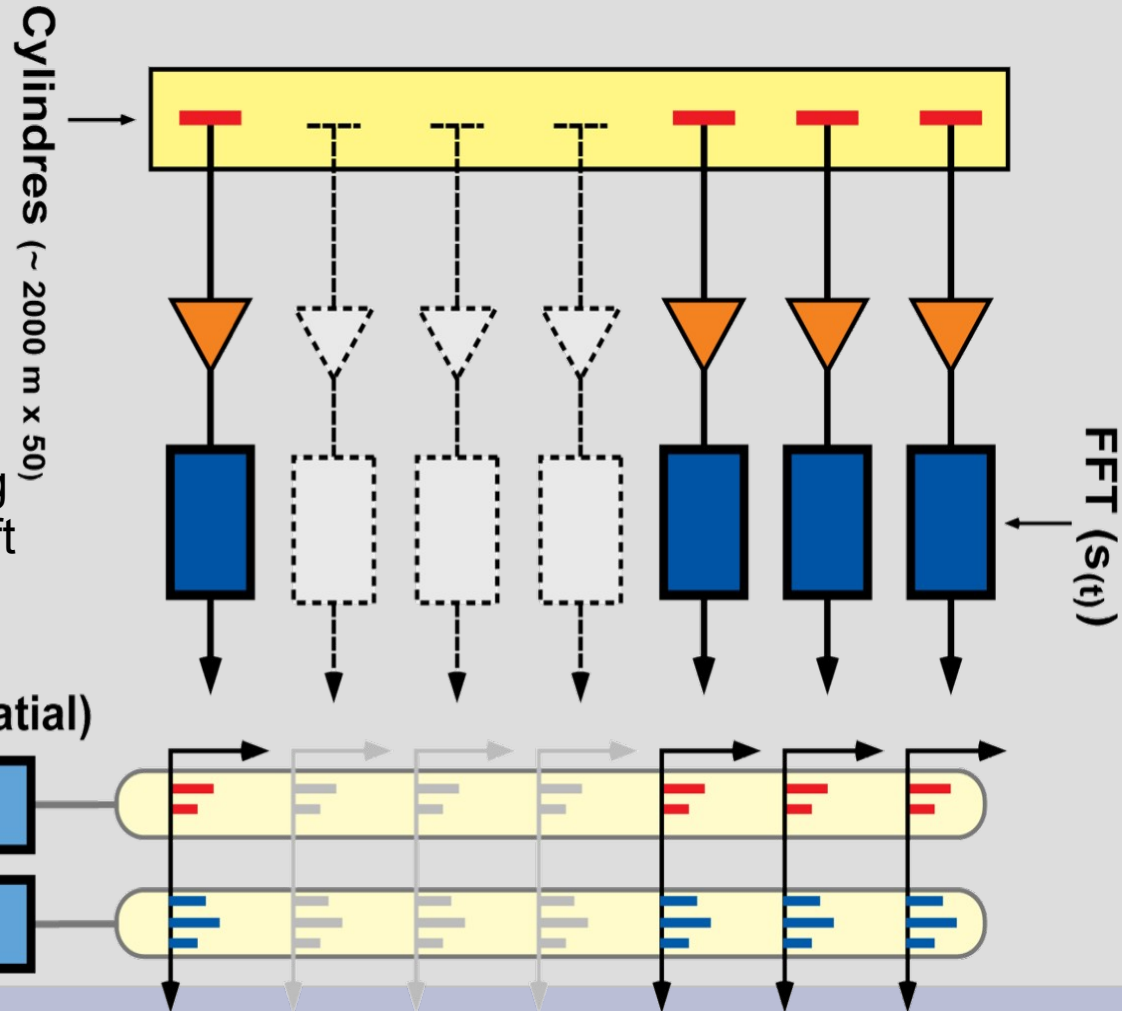
Numerical correlator

- Each channel:
 - Fast Fourier Transform
- ALL channel:
 - Combination of the
 - Same frequency

3 dimensions:
2 angles : FFT beam forming
Distance : frequency red-shift

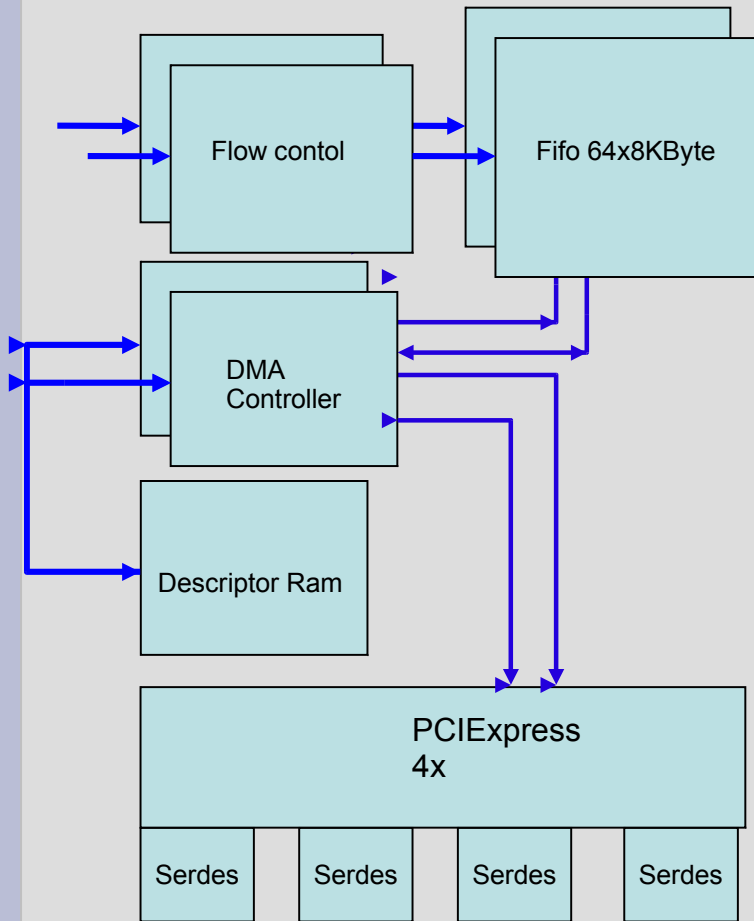
Reconstitution
de lobes sur le ci
pour chaque fréquence

Beam forming
For each FFT
frequency





FPGA synoptic: PCIExpress interface



- FIFO buffering
- Scatter-gather DMA
- PCIExpress:
 - End point
 - 4X

System On Programmable Chip module

The screenshot shows the Altera SOPC Builder interface. The top window displays the system configuration, including the device family (Stratix II GX) and the clock settings (125.6 MHz). The bottom window shows the connections between the modules, including the PCIExpress Controller, onchip_mem, dma_1, fifo, and timing_adapter.

Name	Source	MHz
clk	External	125.6
cal_clk	External	125.6

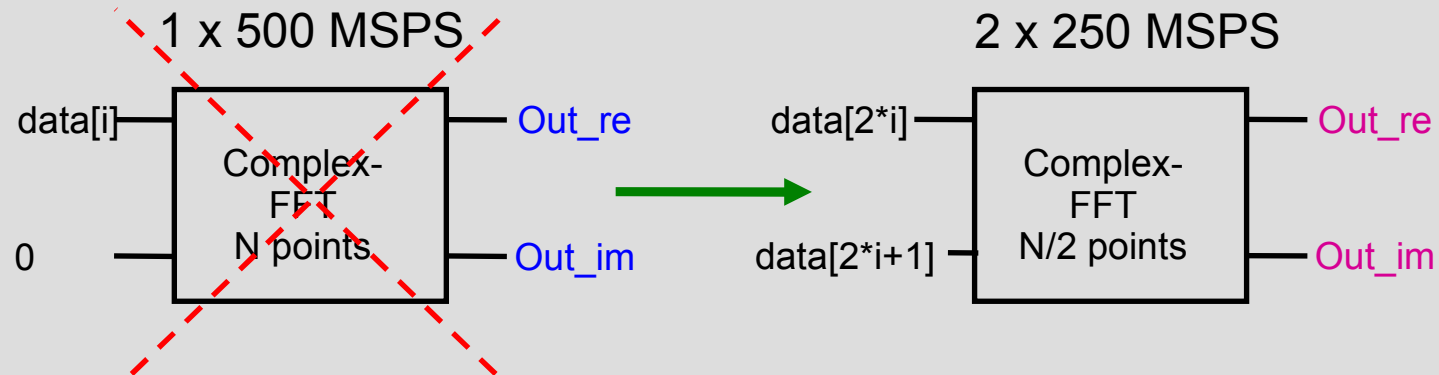
Module Name	Description	Clock	Base	End	IRD
pci_express_controller	PCIExpress Controller	cal_clk			
bar1_0_prefetchable	Avlon Memory Mapped Master	clk	0x00000000	0x00003FFF	
bar2_0_prefetchable	Avlon Memory Mapped Master	clk	0x00000000	0x00003FFF	
control_register_acc	Avlon Memory Mapped Slave	clk	0x00000000	0x00003FFF	
tc_interface	Avlon Memory Mapped Slave	clk	0x00000000	0x00003FFF	
onchip_mem	On-Chip Memory (RAM or ROM)	clk	0x00004000	0x00004FFF	
st1	Avlon Memory Mapped Slave	clk	0x00005000	0x00005FFF	
dma_1	Scatter-Gather DMA Controller	clk	0x00005000	0x00005FFF	
csr	Avlon Memory Mapped Master	clk	0x00005000	0x00005FFF	
descriptor_read	Avlon Memory Mapped Master	clk	0x00005000	0x00005FFF	
descriptor_write	Avlon Memory Mapped Master	clk	0x00005000	0x00005FFF	
m_write	Avlon Memory Mapped Master	clk	0x00005000	0x00005FFF	
in	Avlon Streaming Sink	clk	0x00005000	0x00005FFF	
onchip_mem_1	On-Chip Memory (RAM or ROM)	clk	0x00006000	0x00006FFF	
dma_1	Scatter-Gather DMA Controller	clk	0x00006000	0x00006FFF	
csr	Avlon Memory Mapped Master	clk	0x00006000	0x00006FFF	
descriptor_read	Avlon Memory Mapped Master	clk	0x00006000	0x00006FFF	
descriptor_write	Avlon Memory Mapped Master	clk	0x00006000	0x00006FFF	
m_write	Avlon Memory Mapped Master	clk	0x00006000	0x00006FFF	
in	Avlon Streaming Sink	clk	0x00006000	0x00006FFF	
fifo	Avlon-ST Single Clock FIFO	clk	0x00005400	0x000054FF	
csr	Avlon Memory Mapped Master	clk	0x00005400	0x000054FF	
in	Avlon Streaming Sink	clk	0x00005400	0x000054FF	
out	Avlon Streaming Source	clk	0x00005400	0x000054FF	
fifo_1	Avlon-ST Single Clock FIFO	clk	0x00005410	0x0000541F	
csr	Avlon Memory Mapped Master	clk	0x00005410	0x0000541F	
in	Avlon Streaming Sink	clk	0x00005410	0x0000541F	
out	Avlon Streaming Source	clk	0x00005410	0x0000541F	
timing_adapter	Avlon-ST Timing Adapter	clk			
in	Avlon Streaming Sink	clk			
out	Avlon Streaming Source	clk			
interface	Avlon Streaming Source	clk			
streaming_in_interface	Avlon Streaming Source	clk			
avlon_streaming_sou...	Avlon Streaming Source	clk			
in	Avlon Streaming Sink	clk			
out	Avlon Streaming Source	clk			
interface_1	Avlon Streaming Source	clk			
streaming_in_interface	Avlon Streaming Source	clk			
avlon_streaming_sou...	Avlon Streaming Source	clk			



Post ADC processing: Temporal FFT

FPGA Implementation of real-FFT using a IP Core:

to save hardware resources, we use a $N/2$ points complex-FFT to compute a N -points real-FFT



the **real** signal $s[i=0:N-1]$ is transformed into a **complex** signal : $c[i] = s[2*i] + j*s[2*i+1]$



Post ADC processing: Temporal real-FFT

2 step computation:

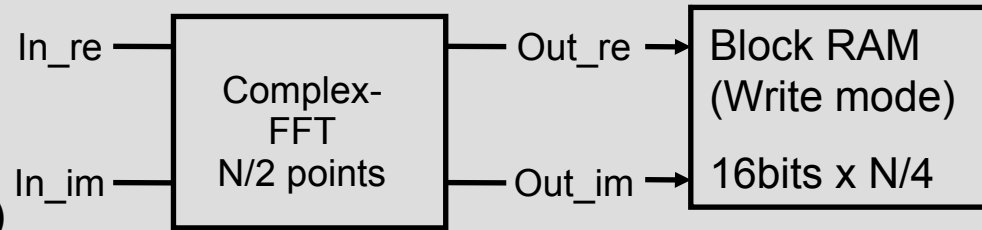
- First step: $N/4$ clock cycles, we feed the block RAM with $FFT_{N/2}(c)[k]$

ADC output:

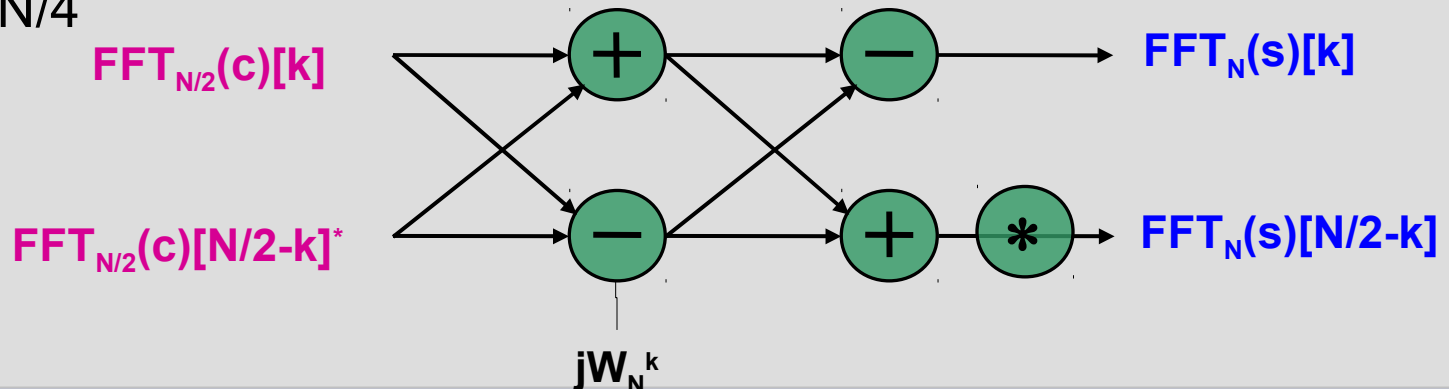
16

bits@250MHz

(2 time samples)



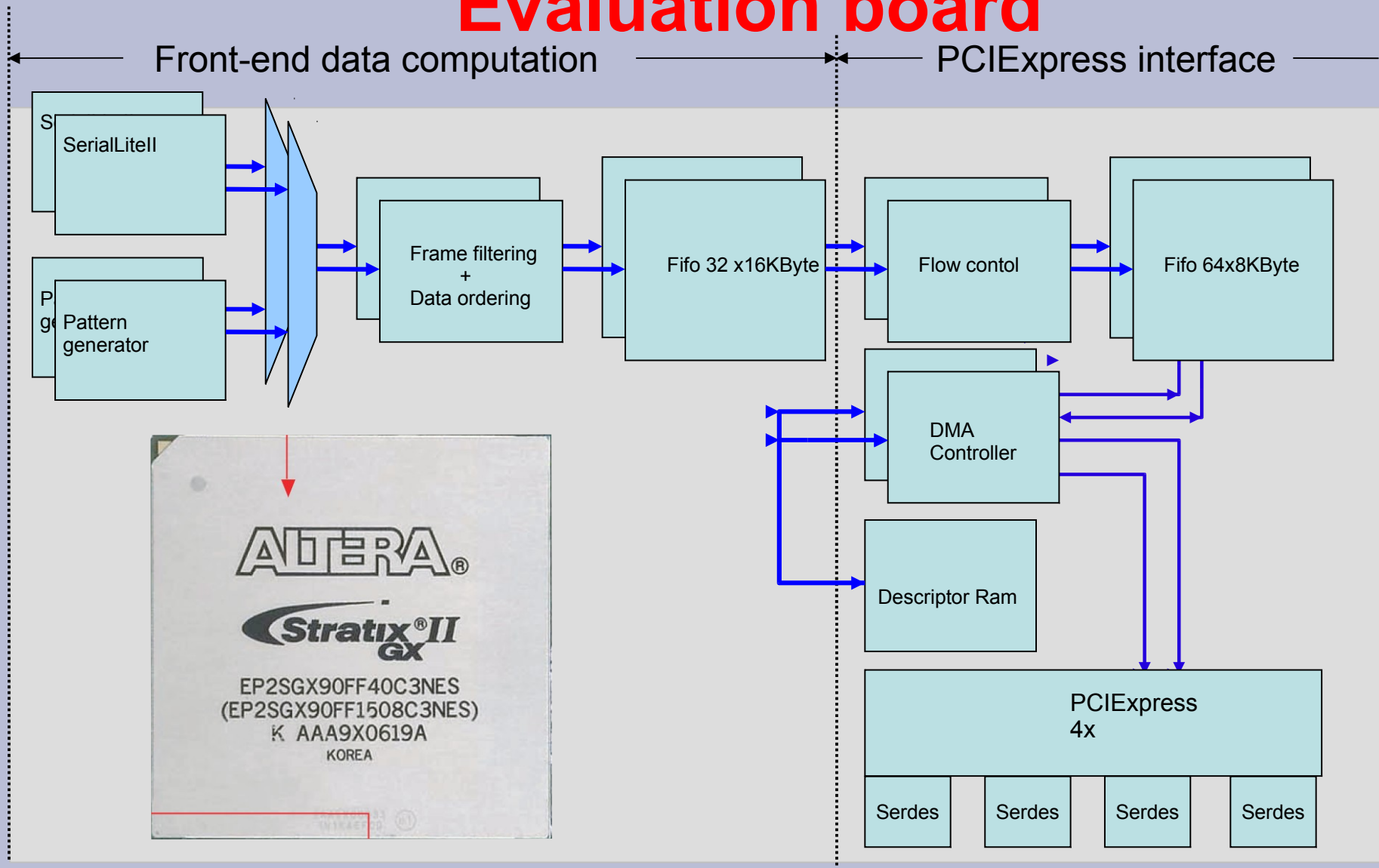
- Second step: $N/4+1$ clock cycles, the output of complex-FFT and data stored in block RAM feed 2 butterfly operators, for $0 \leq k \leq N/4$





Synoptic FPGA PCIeExpress

Evaluation board





ADC board FPGA Synoptic

Firmware:BAO_FFT8192_2ch1000v24,v26

two FFT8k x 8bits transmitted
on one serial link.

