News from FEV_COB

Roman Pöschl

... on behalf of

Funding through:

PHC Star: RECFEB

FKPPL

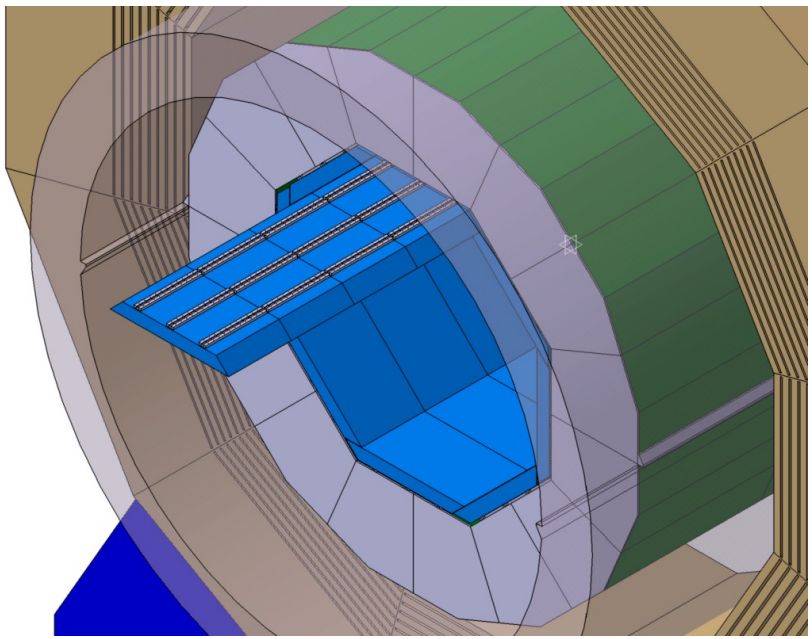
TYL/FKPPL Annual Meeting IPHC/Strasbourg – May 2017

SiW ECAL for a future LC

- SiW ECAL is baseline for future LC detectors

➡ Optimized for Particle Flow Algorithm

Jet energy resolution 3-4%, Excellent photon-hadron separation
Remark: New kid on the block – Timing



The SiW ECAL in the ILD Detector

Basic Requirements:

- Extreme high granularity
- Compact and hermetic (inside magnetic coil)

Basic Choices:

- Tungsten as absorber material

X_0=3.5mm, R_M=9mm, Θ_T=96mm

Narrow showers

Assures compact design

- Silicon as active material

Support compact design

Allows for pixelisation

Robust technology

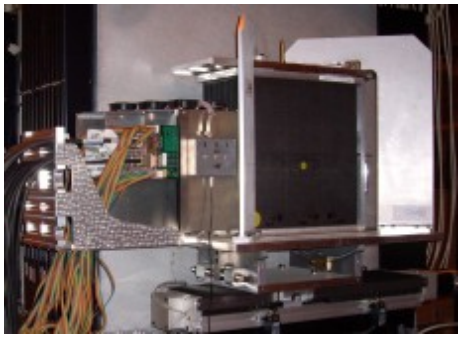
Excellent signal/noise ratio: ~10

SiW ECAL for a future LC

Physics Prototype

Proof of principle

2003 - 2011



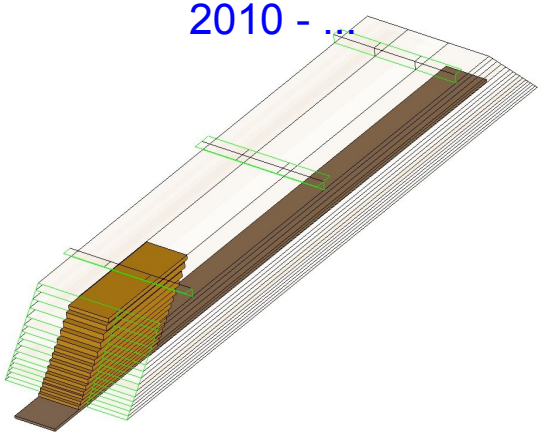
Number of channels : 9720

Weight : ~ 200 Kg

Technological Prototype

Engineering challenges

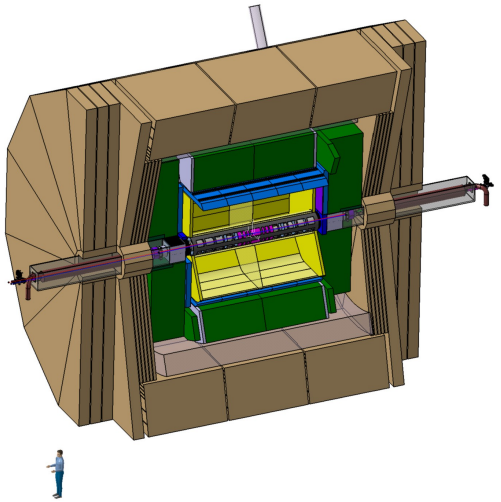
2010 - ...



Number of channels : up to 45360

Weight : ~ 700 Kg

LC detector



ECAL :

Channels : ~100 10^6

Total Weight : ~130 t

All well integrated in international collaborations as CALICE, AIDA-2020 and the Linear Collider detector concept

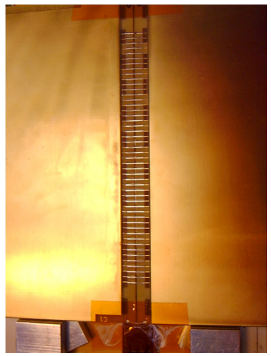
CALICE/LC R&D spawned off to LHC detectors (CMS, ATLAS and since recently also LHCb)

More details see talk by Vincent Boudry on Thursday morning

SiW ECAL – Long layer

A layer is composed of several short ASUs:

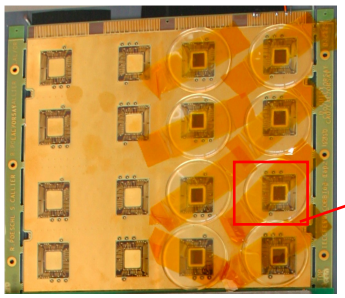
- A.S.U. : Active Sensors Units
- Similar layout for ATLAS HGTD

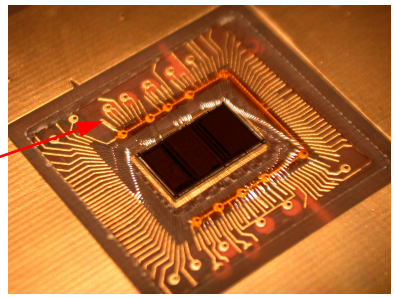


Interconnection with Flat flexible cable

ASIC+PCB+SiWafer =ASU, 18x18cm²

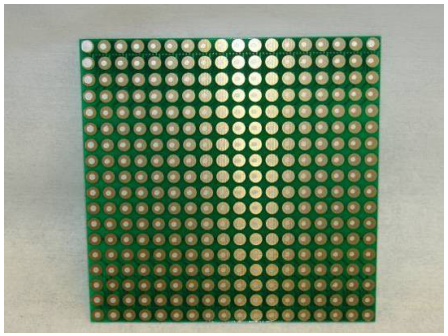
Wire Bonding or BGA





PCB is glued onto SiWafers

using a gluing robot



Some key numbers:
~10000 readout pads
~10000 interconnections
Current peaks >10 A for 2ms
Reliable signal propagation to be assured
Further details in backup

Successful realisation of a long layer is maybe one of the most challenging R&D projects in worldwide detector R&D

PCB R&D

Two options:

BGA packaged chips

BGA version is safe incremental step:

test of chips before soldering ;

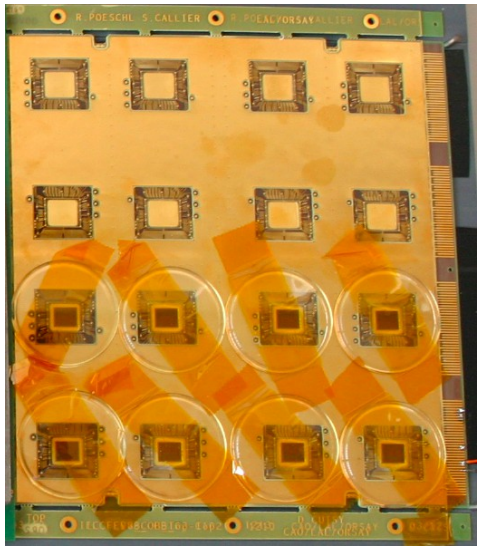
Space for external decoupling capacitors

Symmetric stacking will improve flatness, good for wafer gluing

Optimal shielding of signal traces

Solution for technological prototype

PCB with naked die (Chip-On-Board)



- Thin board (~1.2mm)
  => maximal channel density

- Tests since 2015
  => Intensive test programme
  e.g. Noise and cross talk

- New production for 2017

Our Korean Partner ITAEC@SKKU

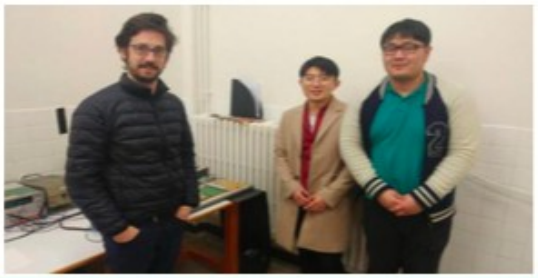
- **ITAEC-ILC Group at LAL Collaborative Research PROGRAMME**
  -internship to train for operating readout-electronic prototypes(6/3/2017~30/3/2017)

- ✓ **ITAEC(IT Accelerator Engineering Center) at SKKU**
- ✓ Pf.Chai
- ✓ Leader of ITAEC

Huisu Kim
PhD in EEE at SKKU

Working with Roman, Adrian, Stephane and Remi

Bokyeom Kim
Master in EEE at SKKU

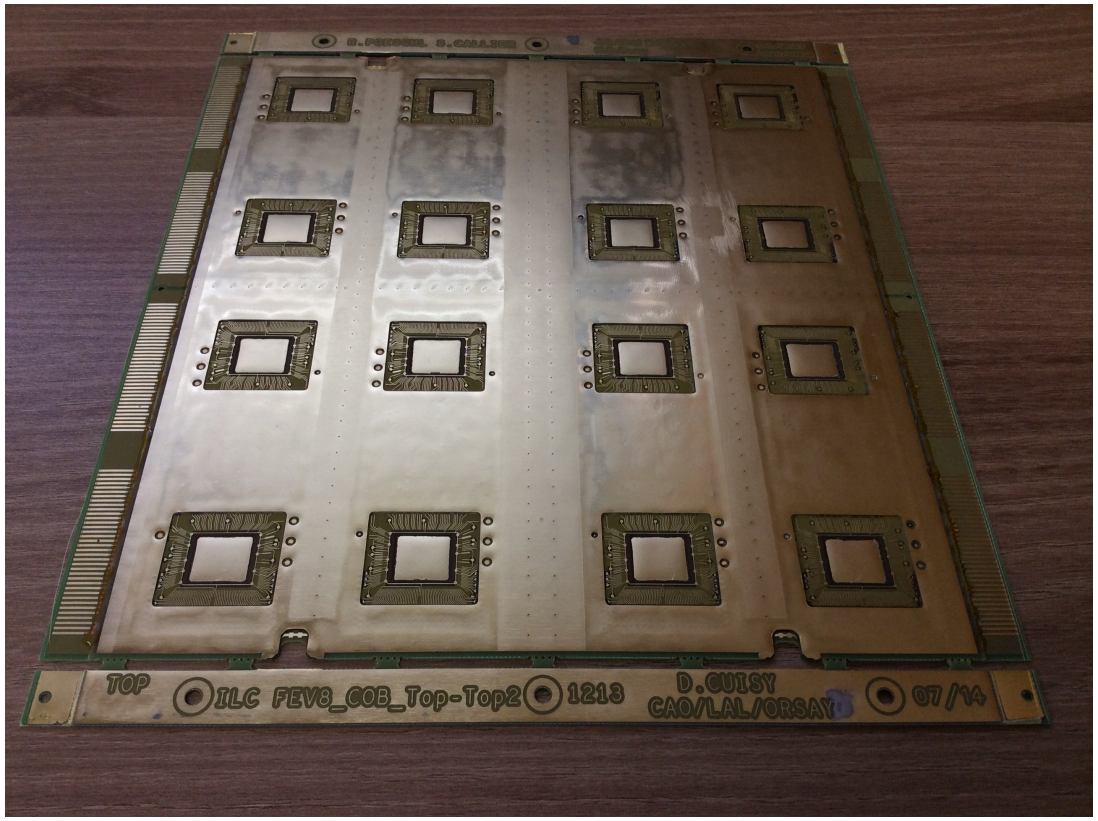


+ Master student EEE Woojung Jun

FEV8_COB

- Produced by EOS Company South-Korea under supervision of SKKU/OMEGA/LAL
  10 board production autumn 2014, Four boards sent to LAL
- 3 Boards wire bonded at CERN in March 2015 and February 2016

- First debugging series at LAL in Summer/Autumn 2015



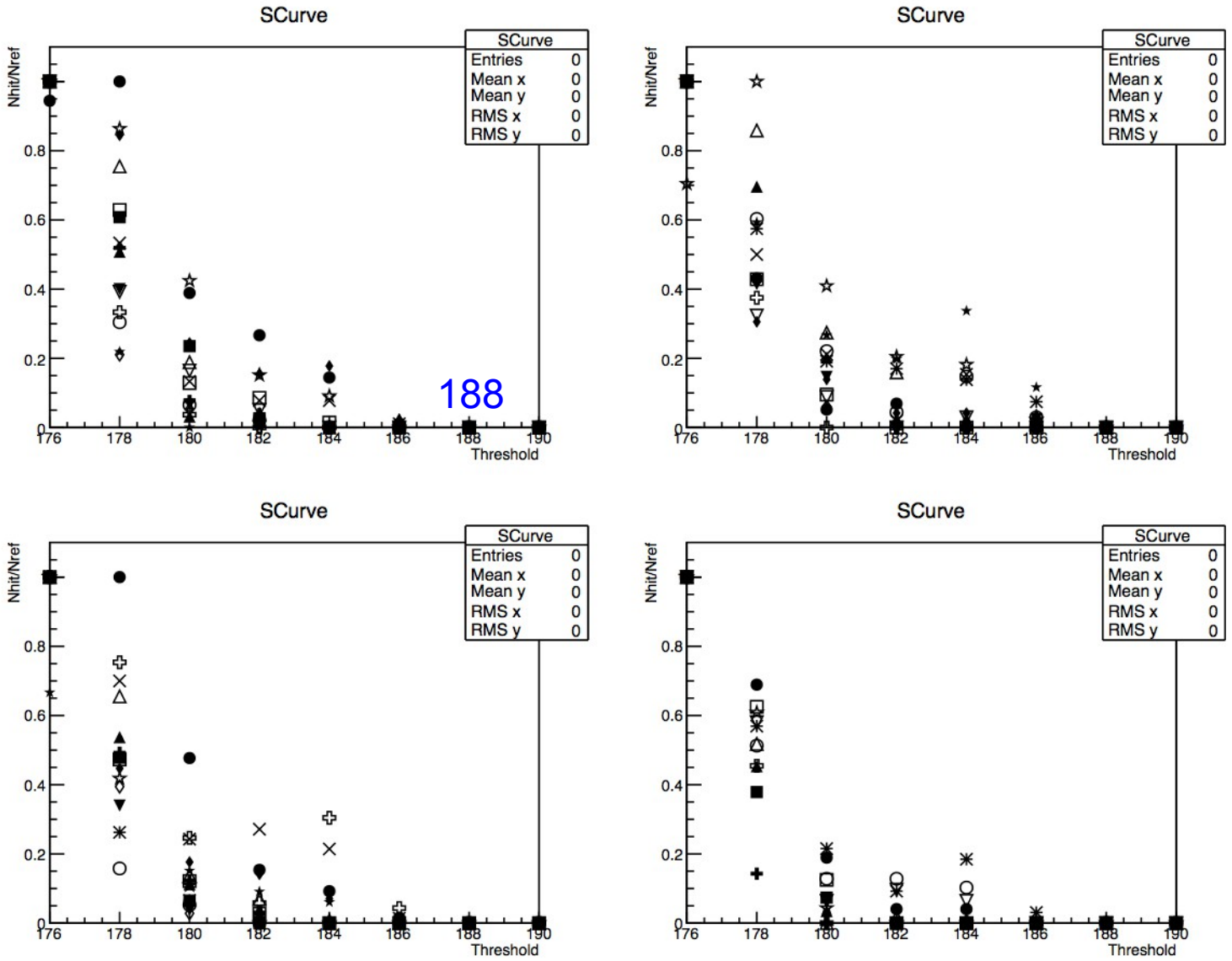
Support by:

LPNHE

Results from test campaign – Spring 2016 I

S-Curves ASIC0:
w/o charge injection

S-Curve obtained
by a sucessive
lowering of
ASIC Trigger threshold

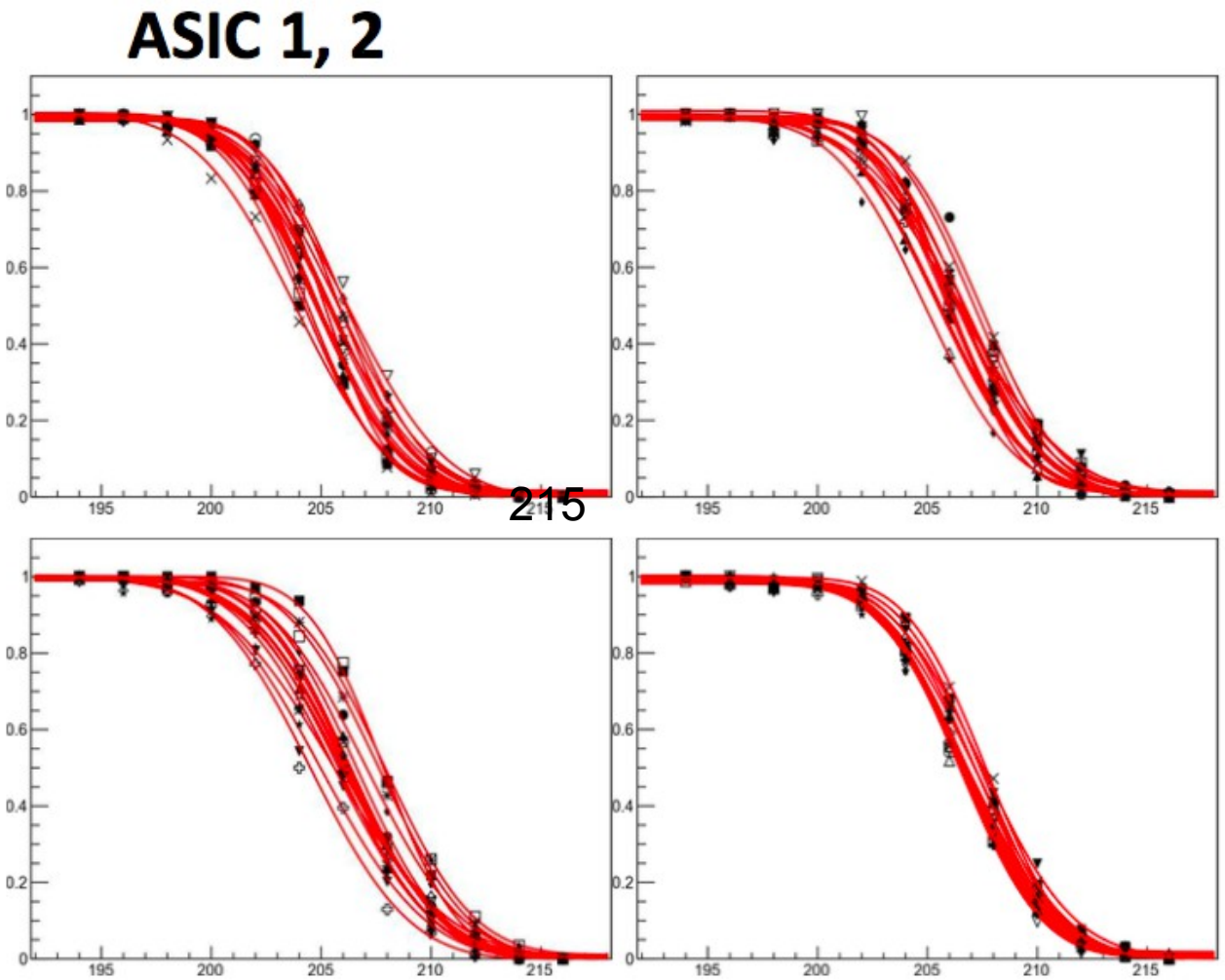


In general rather smooth behaviour even w/o charge injection
some disabled channels though

Studies by
A. Chamseddine
NPAC Internship 2016

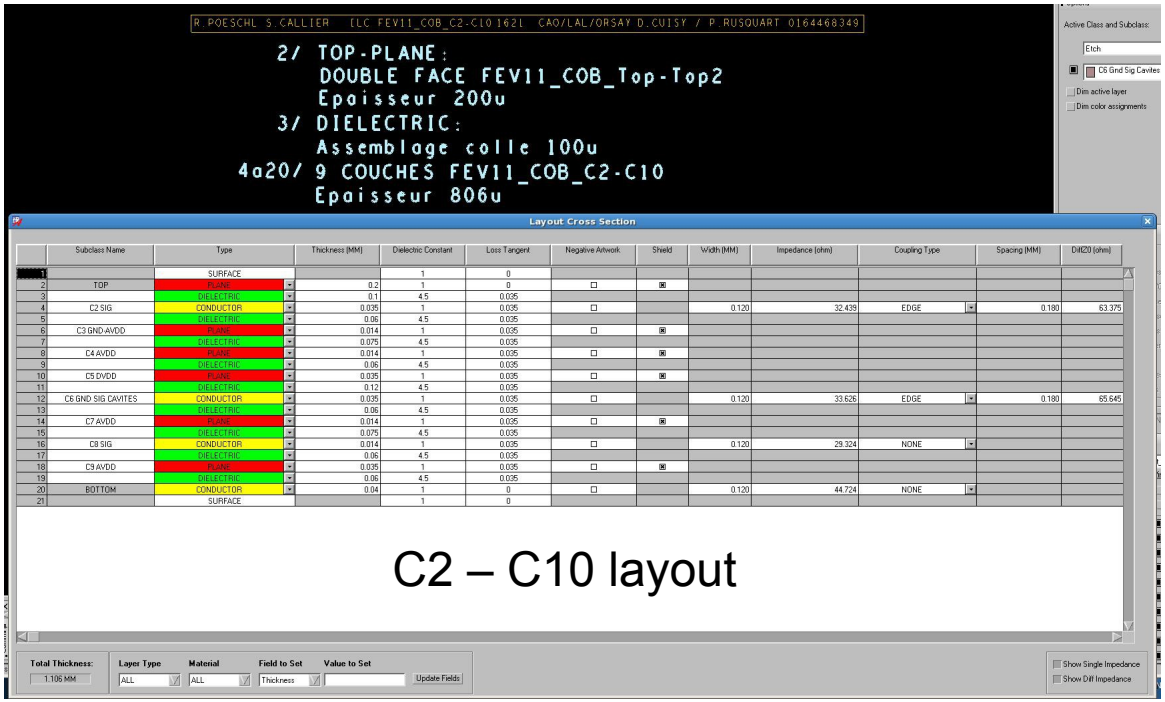
Results from test campaign – Spring 2016 II

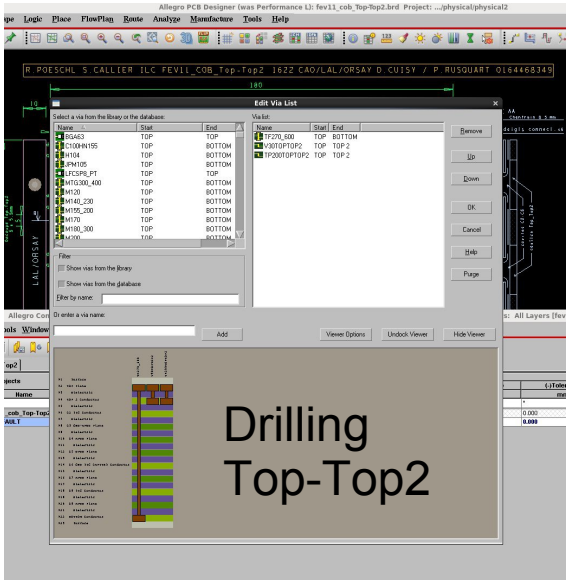
S-Curves ASIC3:
with charge injection
~2 MIP

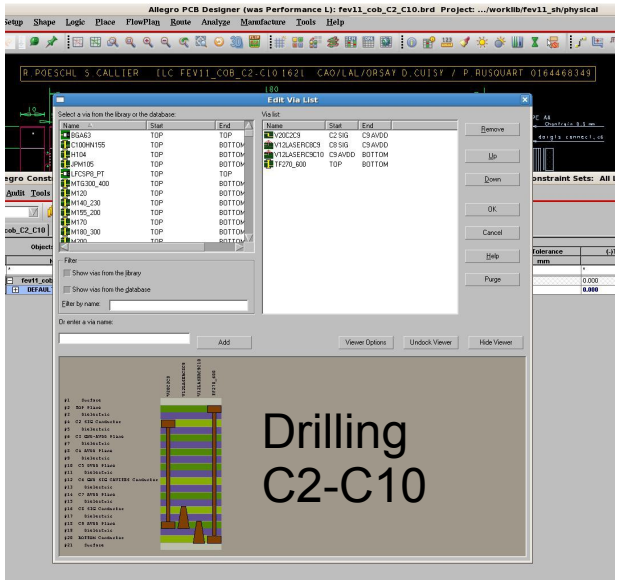


- Tests carried out in 2015 and 2016 revealed no show stopper
- FEV8 design is however outdated, need to get in phase with current development
- FEV8_COB -> FEV11_COB

FEV11 Design Phase

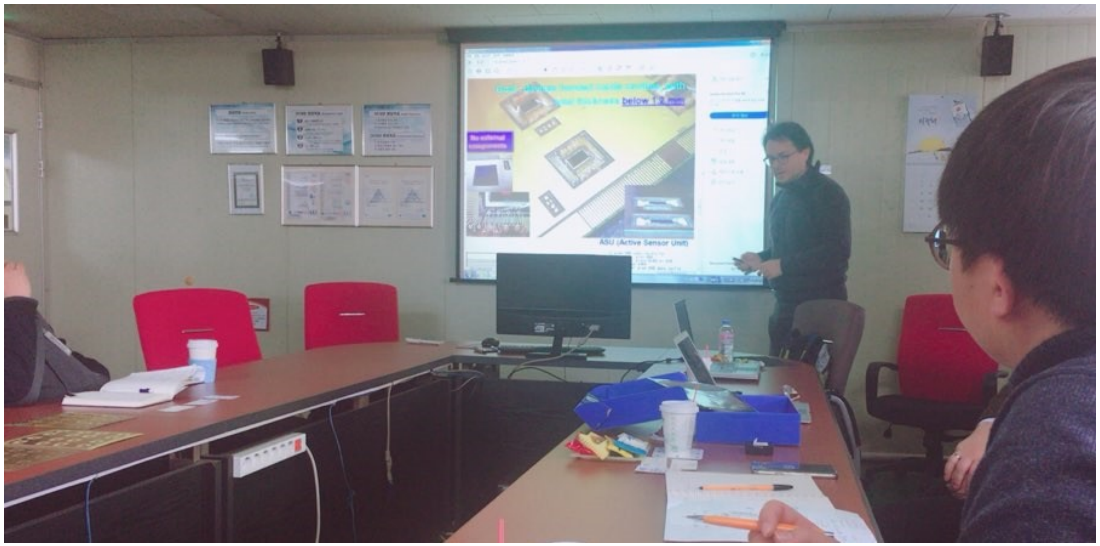






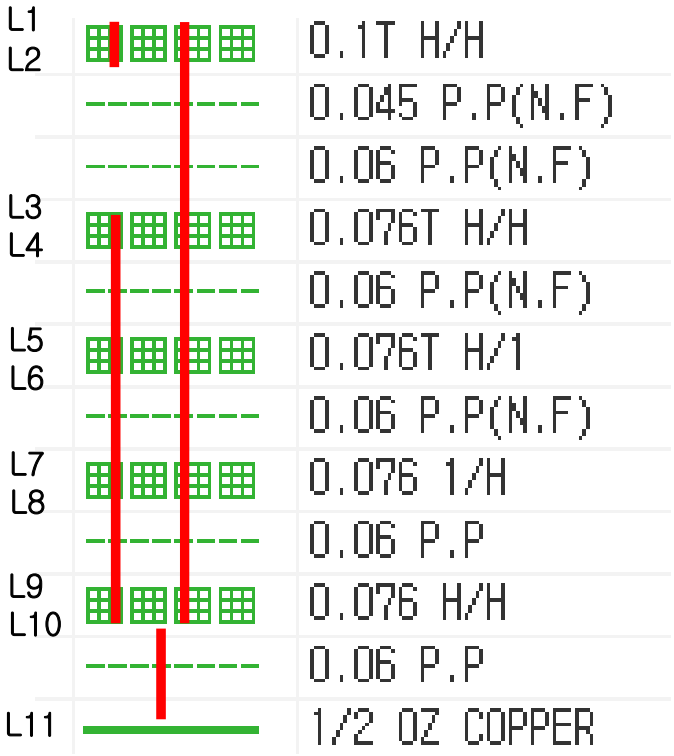
- Design by Stephane Callier and Pascal Rusquart (LAL)
- Iterations during Summer 2016
- Broadly speaking FEV_COB Is a compilation of two boards Top-Top2 C2 - C10 (Glued together)
- Sent to EOS in December 2016

Meeting(s) with EOS – May 2016 and January 2017



- Organised through SKKU (Thanks to Prof. Chai, Woojung, Mitra ...)
- Intensive discussion to understand our requirements
  - Thin board, flat board ...
- May 2016 – Feedback on experience with FEV8_COB and first discussion on FEV11_COB
- January 2017 – Launch of FEV11 production

Exchange with EOS

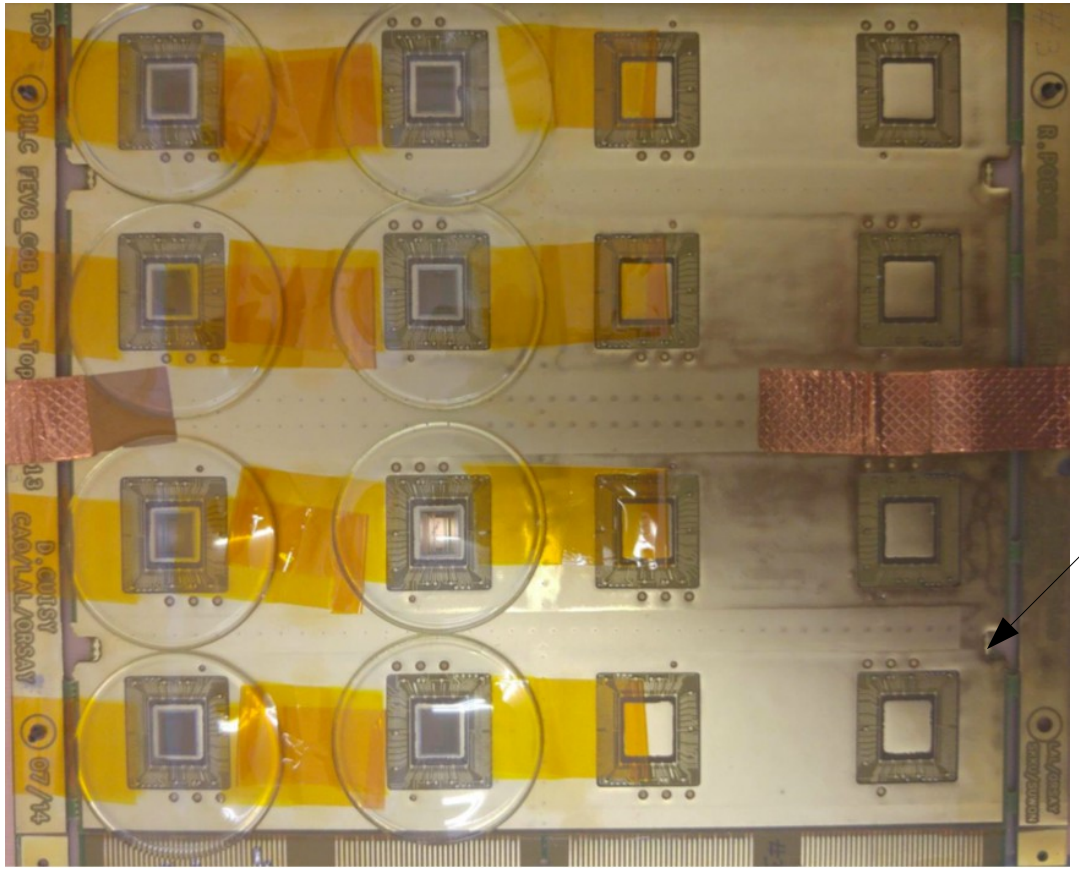


- Excellent communication with EOS company
- E.g. Proposal by EOS on wire drilling
  May prevent to have two glued boards
  Two glued boards was issue of discussion with French/European providers back in ~2011

  => Optimised mechanical features!?
- Board is under production now
- Expect delivery of FEV11_COB during Spring/Summer 2017

- In total 1.11mm thickness
- We “allowed” them to go thicker (up to 1.5mm) if this in beneficial for the mechanical features

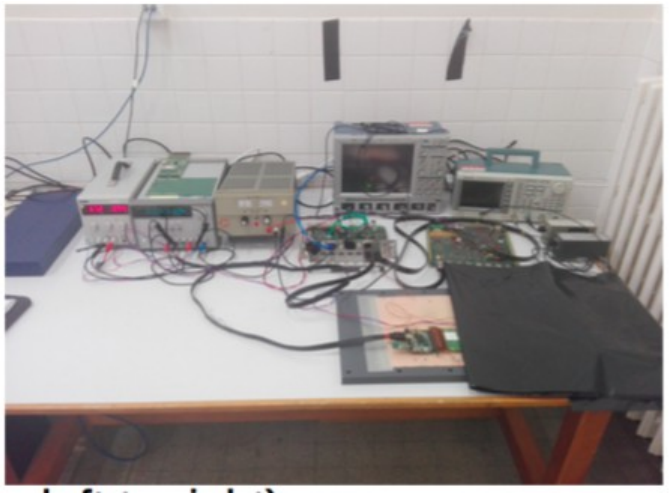
FEV_COB Gluing – Some remarks

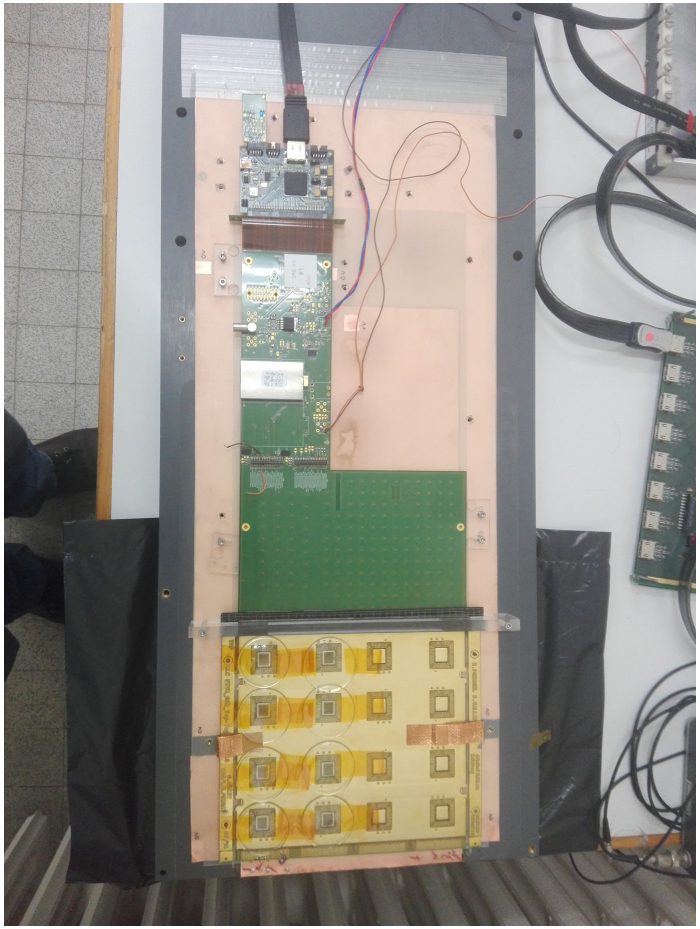


- Adequacy for gluing will have impact on design
- In general flat surface should be beneficial for application of robot
  Devil is in the details
- e.g Probe point may need to be replaced to assure aspiration
- Submission of new FEV11_COB scheme happened taking into account observations gluing experts
  (N.B.: and assembly experts of course)

Two meetings on gluing aspects of FEV_COB at LPNHE during autumn

FEV_COB Testbench at LAL

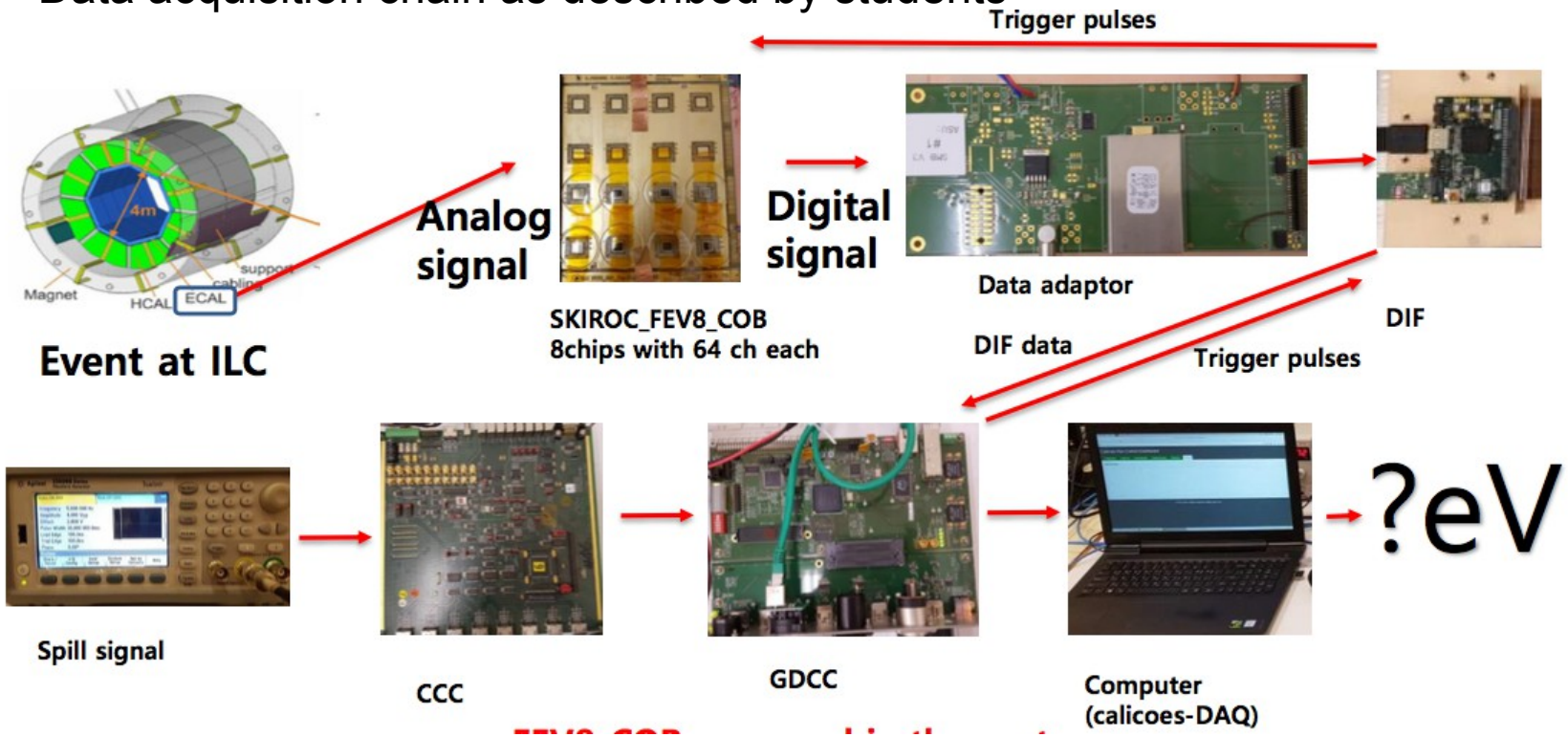




- Update of test bench
  - LDA -> GDCC
  - Calicoes/Pyrame v.before the war -> Recent version
  - Firmware update
- Update realised by Team of LAL, LLR, OMEGA ... THANKS
- Used for training of two students from SKKU Bokyeom Kim and Husui Kim
- Testbench will be shipped to SKKU in the coming two weeks (some delay due to other business, sorry)

Training at LAL

- Data acquisition chain as described by students



- Training implied switch to updated DAQ hardware
  Devil is in the details, nice trigger curves towards the end of training

- Problems have the “advantage” that one goes into the details of a system

FEV_COB Next steps

- Tests with FEV8_COB revealed no show-stoppers
  - Option to equip FEV8_COB with baby wafers but I rather prefer to phase it out
- Production of new PCBs on going
  - Move from FEV8 -> FEV11 scheme
  - Expect delivery towards end of Spring/beginning of Summer 2017
- Meetings with EOS company in May 2016 and January 2017
  - Emphasis on mechanical properties
  - Revision of metallisation of bonding pads (Check General Metal Finishing)
- All Korean solution requires finding a bonding company
- Migration to new DAQ Hardware
  - Material for test benches LAL and SKKU,
  - SKKU students were trained at LAL
  - Shipment of testbench to SKKU imminent
- FEV11_COB and DAQ update will allow for smooth integration of COB in regular beam test stacks
  - Including tests at SKKU 6 MeV electron linac or MeV ITAEC proton cyclotron

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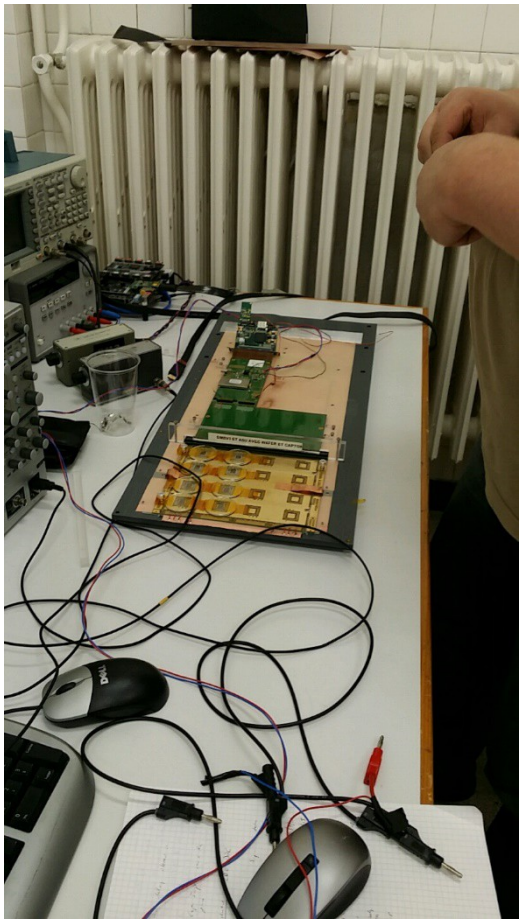
Backup

FEV_COB Team – September 2015

Intensive debugging during September 2015

Visit of two students from SKKU and one from Kyushu, possible thanks to FKPPL

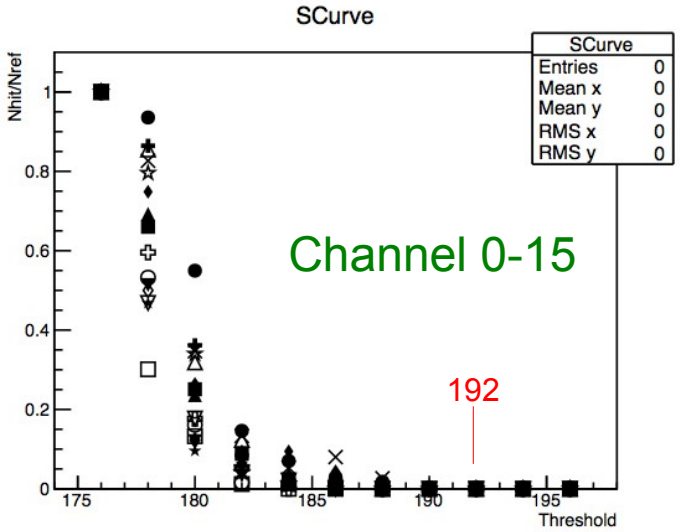


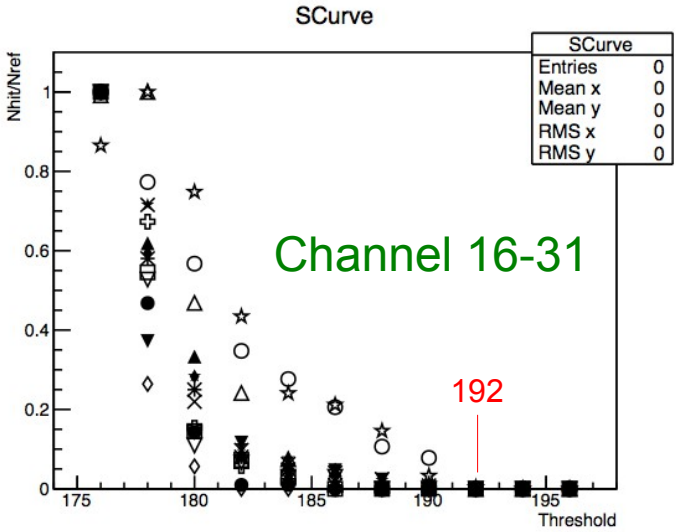
Team from SKKU (Korea), OMEGA, LAL and Kyushu

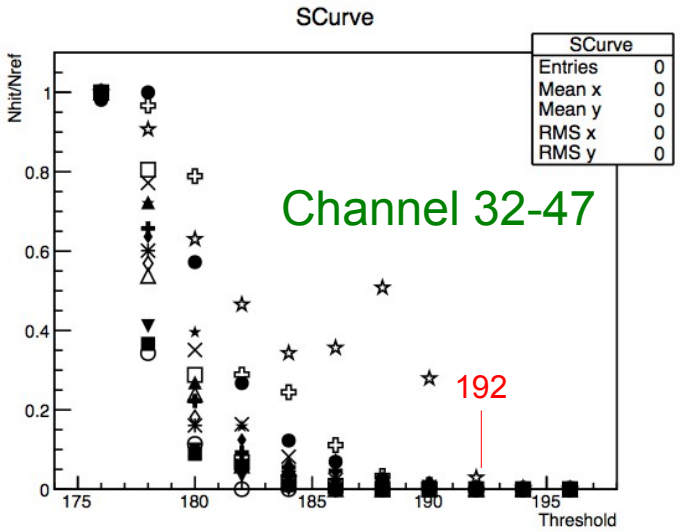
Particular thanks to Hiroto for helping to get the SKKU team going!!!!

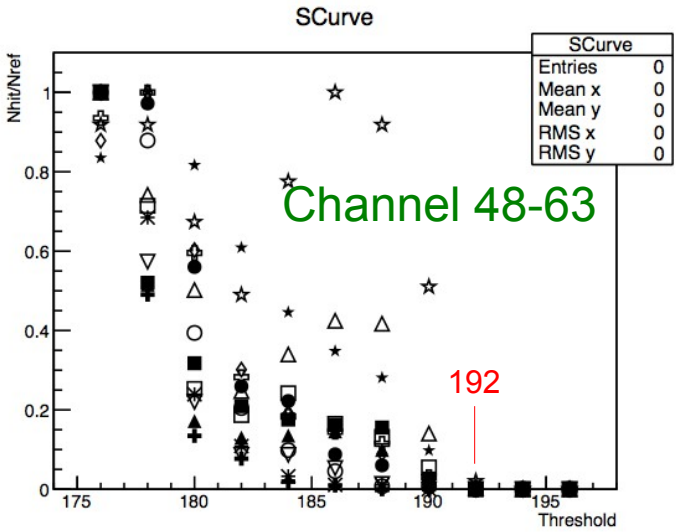
The first S-Curves – August 2015

Chip0 after disabling of 7 channels: No charge injection









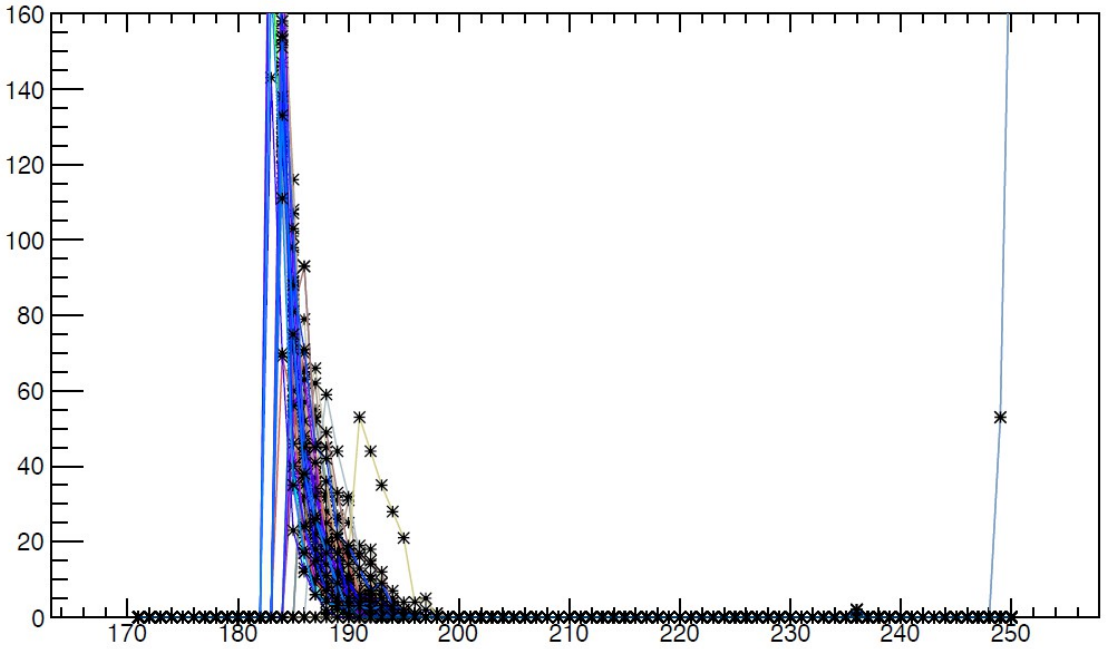
- S-Curves for Chip0 look reasonable up to excellent

- 192 DAC Counts is Common threshold for this ASIC (~1 – 1.5 MIPs)

- Remark: Tests with a better shielded Setup

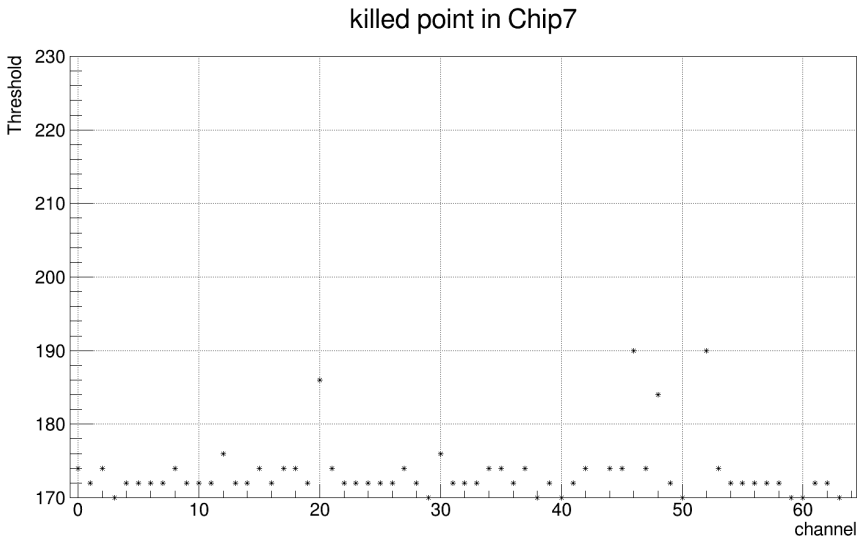
  -> 5-10 DAC counts smaller threshold

Measurements by Kyushu and SKKU – September 2015



W/o electrical shielding:

Typical DAC threshold
185 DAC Counts



W/o impoved shielding:

Typical DAC threshold
~170 DAC Counts

FEV_COB Funding Situation

- P2IO Project HIGHTEC (France)
  - 25kEUR for thin PCBs and DAQ Setup

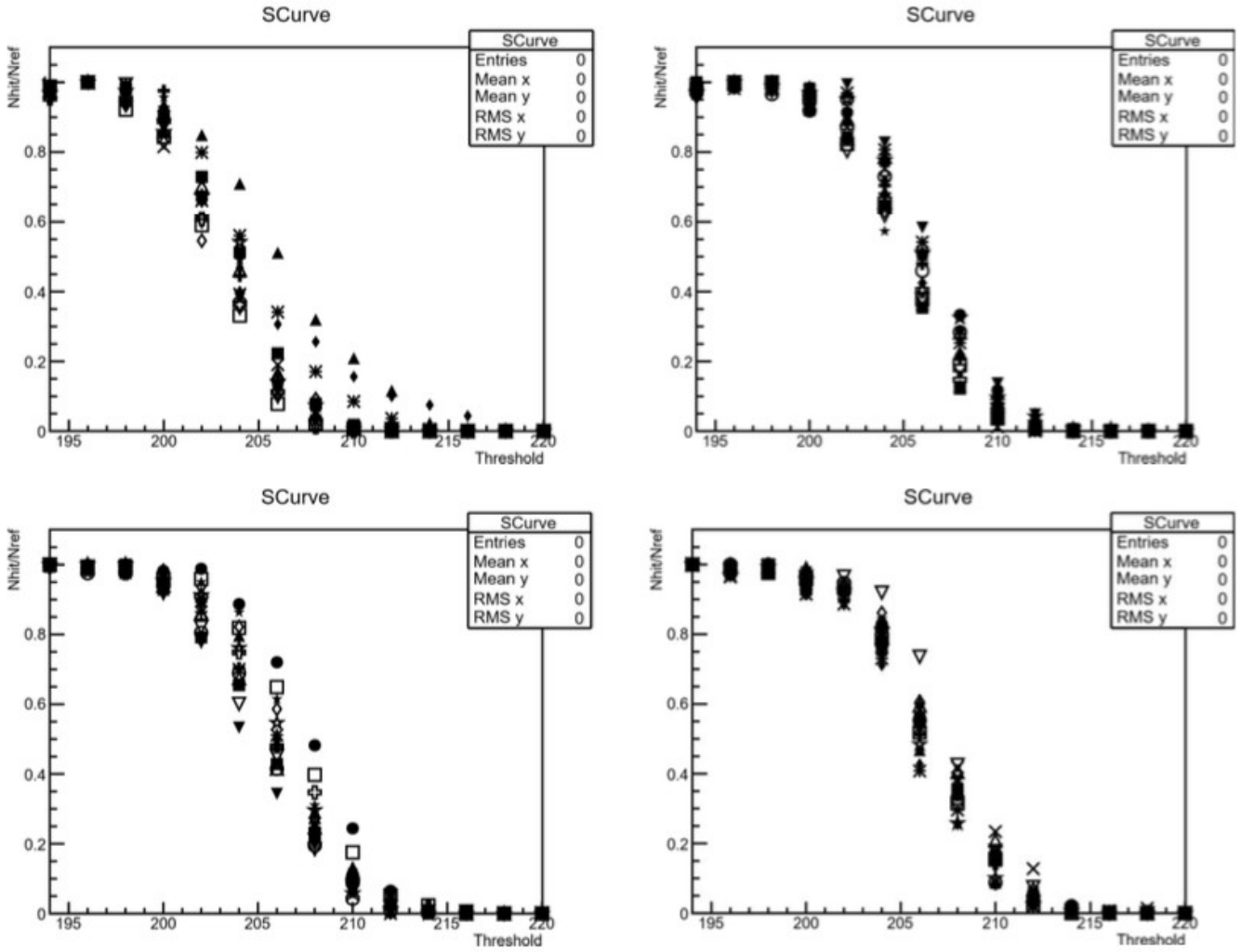
- AIDA2020
  - Some money for new DAQ development (new hardware available ~mid-2017)

- PHC Star for travel
  - 16 kEUR (France), 30kEUR (Korea)

- FKPPL for travel
  - Funding to be decided at this FKPPL Meeting

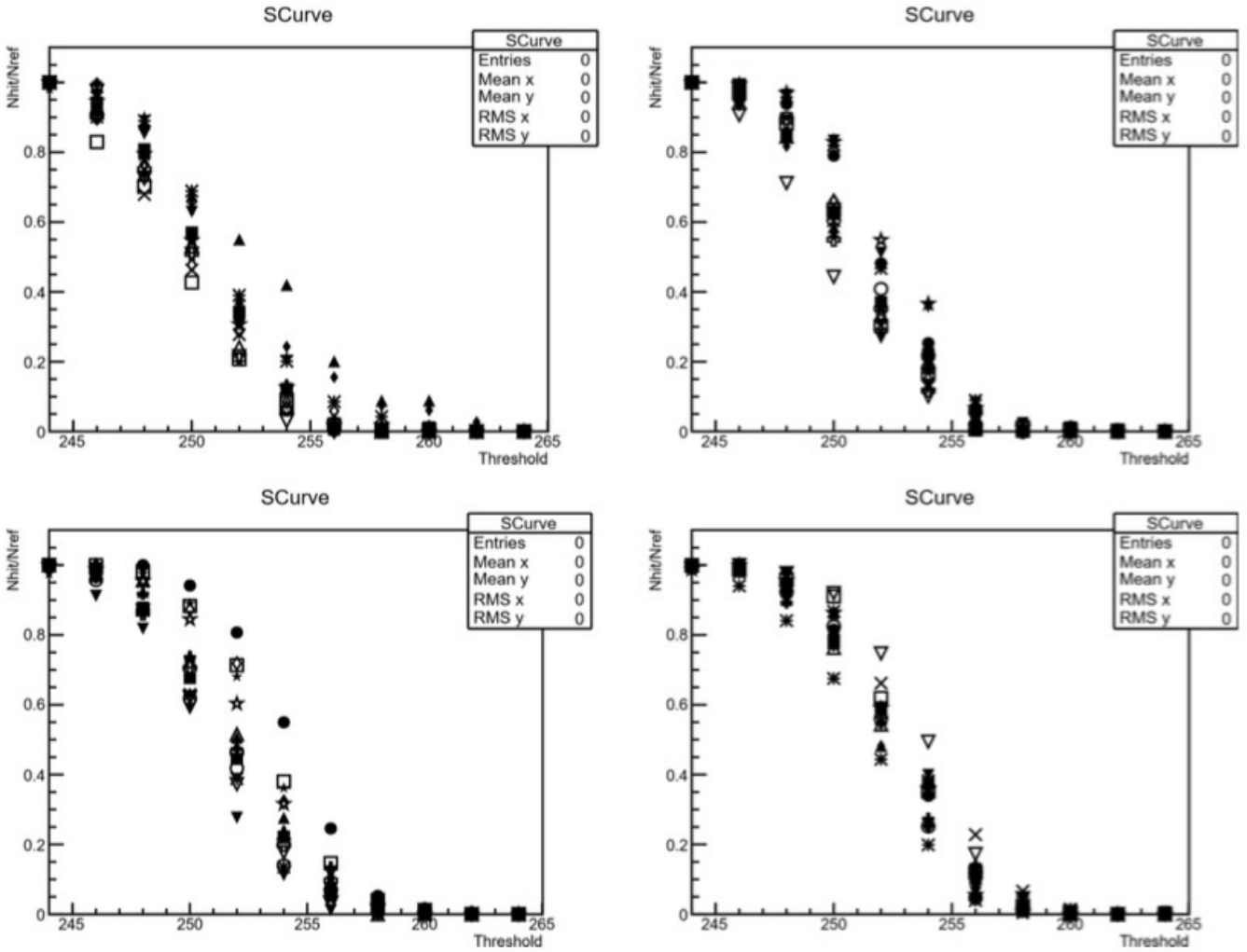
Results from test campaign – April 2016 IV

S-Curves ASIC3:
with charge injectio
~2 MIP



Results from test campaign – April 2016 V

S-Curves ASIC3:
with charge injection
~5 MIP



Results from test campaign – April 2016 III

List of excluded cells

	Channels	Test
ASIC 0	11, 17, 30, 52, 63	High Threshold Trigger
	44, 51, 55, 57	S-curves without Signal Injection*
	47	10 MIP Signal Injection
ASIC 1	30, 38	High Threshold Trigger
	22, 27	S-curves without Signal Injection*
	48	10 MIP Signal Injection
ASIC 2	30, 38	High Threshold Trigger
	21, 27	S-curves without Signal Injection*
	48	10 MIP Signal Injection
ASIC 3	0, 4, 45, 56	High Threshold Trigger
	2, 7, 11, 13, 20, 63	S-curves without Signal Injection*
	47	10 MIP Signal Injection
ASIC 4	7, 18	High Threshold Trigger
	9, 13, 17, 28, 30, 36, 61	S-curves without Signal Injection*
	48, 50	10 MIP Signal Injection
ASIC 5	26, 30	High Threshold Trigger
	53	S-curves without Signal Injection*
	47	10 MIP Signal Injection
ASIC 6	26, 30	High Threshold Trigger
	7, 8, 9, 10, 13, 14, 35	S-curves without Signal Injection*
	47	10 MIP Signal Injection
ASIC 7	46 , 52	High Threshold Trigger
	20, 24, 33, 37, 38, 42, 44, 48	S-curves without Signal Injection*
	51**	10 MIP Signal Injection