SOI Monolithic Pixel Detector Technology

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Outline

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II. SOI Pixel Process
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Compton Electrons Tracks
I. Introduction

SOI technology is a natural solution in the evolution of radiation pixel sensor.
Silicon-On-Insulator Pixel Detector (SOIPIX)

Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.
Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only. → High reliability and Low Cost.
- High Resistive fully depleted sensor (50um~700um thick) with Low sense node capacitance. → Large S/N.
- On Pixel processing with CMOS circuits.
- No Latch up and very low Single Event cross section.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.
First SOI Wafer (SIMOX)

First good quality SOI wafer
SIMOX (Separation by Implanted Oxygen)

This took long implantation time of Oxygen, so the production cost was very high and applications are limited.

Oxygen Ion Implantation
120-200 keV, 4-20×10^{17} cm^{-2}

Si Substrate (Handle Wafer)

Si Overlayer

Buried Oxide Layer

annealing
3-6 hours
~1300 °C

Si Substrate (Handle Wafer)

K. Izumi (NTT Japan, 1978)
Present SOI Wafer (SmartCut™)

Become popular after 2000.

CMOS (Low R)

Sensor (High R)

Layer Transfer

Michel. Bruel (Leti, 1991)

(from SOITEC Web)
II. SOI Pixel Process
To use SOI technology for pixel detector is already discussed in 1990(*).

Issues in SOI Pixel

- Transistors does not work with Detector High Voltage. *(Back-Gate Effect)*
- Circuit signal and sense node couples. *(Signal Cross Talk)*
- Oxide trapped hole induced by radiation will shift transistor threshold voltage. *(Radiation Tolerance)*

Unfortunately, in 1990s, due to immature process technology, no good high-resistivity SOI wafer etc., many SOI sensor R&D projects were stopped.
- Cut Top Si and BOX
- High Dose

- Suppress the **Back Gate Effect**.
- Shrink pixel size without losing sensitive area.
- Increase breakdown voltage with low dose region.
- Reduce electric field in the BOX which improves radiation hardness.
Back-gate effect is completely suppressed by the BPW.
## Lapis Semi.\(^(*)\) 0.2 μm FD-SOI Pixel Process

| Process | 0.2μm Low-Leakage Fully-Depleted SOI CMOS  
1 Poly, 5 Metal layers.  
MIM Capacitor (1.5 fF/um\(^2\)), DMOS  
Core (I/O) Voltage = 1.8 (3.3) V |
|----------|-------------------------------------------------------------------------------------------------|
| SOI wafer (single) | Diameter: 200 mm\(\phi\), 720 μm thick  
Top Si : Cz, \(~18 \Omega\text{-cm}, \text{p-type}, \sim40 \text{ nm thick}  
Buried Oxide: 200 nm thick  
Handle wafer: Cz (n) \(~700 \Omega\text{-cm},  
\text{FZ}(n) > 2k \Omega\text{-cm}, \text{FZ}(p) \sim25 \text{ k} \Omega\text{-cm etc.} |
| Backside process | Mechanical Grind, Chemical Etching, Back side Implant, Laser Annealing and Al plating |

\(^(*)\) Former OKI Semiconductor Co. Ltd.
We operate Multi-Project Wafer (MPW) run. (1~2 times/year)

Only one SOI radiation pixel process in the world!
Issues in SOI detector

Sensor and Electronics are located very near. This cause ...

Then we introduced additional conductive layer under the transistors (Double SOI).
Double SOI Detector
• Middle Si layer shields coupling between sensor and circuit.
• It also compensate E-field generated by radiation trapped hole.
• Good for Complex function and Counting-type sensor.
• Can be used in High radiation environment.
Cross section of the Double SOI Pixel

- Transistor
- Middle Si
- Metal 1
- Sensor Contact
- Middle Si Contact
- Metal 5

Scale: x9.0k TE 12/10/16

3.00μm
Effect of Double SOI

Cross Talk from Clock line

Shield:
Cross Talk between Circuit and Sensor is reduced to 1/20.

(by Lu Yunpeng (IHEP))
Gamma-ray Irradiation Test
(Id-Vg Characteristics v.s. SOI2 Potential)

By setting Middle Si potential (Vsoi2) to -5V, Id-Vg curve returned nearly to pre-irradiation value at 100 kGy(Si) (10 Mrad).

(by U. of Tsukuba)
Variation of Id-Vg Characteristics and Effect of SOI2 Potential

PMOS

I/O Normal Vt
Source-Tie
L/W = 0.35μm/5μm

Threshold voltage shift is not so large in PMOS, but Drain Current decreases much.
Major cause of the drain current degradation by radiation is $V_{th}$ increase at gate edge due to positive charge generation in spacer. Charge in spacer control the $V_{th}$ of the parasitic transistor. To reduce this effect, lightly doped drain (LDD) dose should be increased. Present process has rather low dose in LDD region to aiming lower power.
Id-Vg Characteristics in Triode Region

With increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 kGy(Si).

In the SOI process, it is possible to merge NMOS & PMOS Active region and share contacts.
Single Port SRAM Bit Cell

Cell Size: 3.94\( \mu \text{m} \times 3.06\mu \text{m} = 12.06\mu \text{m}^2 \)
Hexagonal Counting-type Pixel (under development)

CNPIX1

Smallest Counting-type Pixel of this kind.
(much smaller than designed in 0.13um process)

Charge Amp +
Shaper +
 Discriminator +
Q Share Handling +
19bit Counter +
7bit register
(in 2,340 um²)
III. Detector Examples
Integration type detector & 3D CT

INTPIX4
Pixel Size: 17 um x 17 um
No. of Pixel: 512 x 832 (= 425,984)
Chip Size: 10.3 mm x 15.5 mm

Sensor: INTPIX4 FZn, Backside Illumination
HV: 200V, Integration Time: 1ms, ScanTime: 320ns/pix, 1000frame/event
KEK PF, X-ray Energy: 9.5keV
Took images for 0~180° at every 1 degree.

(by R. Nishimura, K. Hirano (KEK))
INTPIX4: Computed Tomography with Syncrotron X-ray

(by R. Nishimura, K. Hirano (KEK))
Contrast Transfer Function

Contrast of 16μm Pitch Slit

INTPIX4(17μm pix): 0.57, FPIX(8μm pix): 0.83
ILC Vertex Detector R&D : SOFIST
(SOI sensor for Fine measurement of Space & Time)

Test Chip Spec.
- Chip size: 2.9 × 2.9 mm²
- Substrate (FZ n-type, 2 kΩ cm)
- Pixel size: 20~25 μm
- No. of Pixel: 50 × 50 pixels
- Gain: 32 mV/ke- (Cf=5fF)
- Analog signal memories: 2 for signal or 2 for time
- Column-ADC: 8 bit
- Zero Suppression Logic

R&D for 3D integration is also progressing.
120GeV/c Proton Beam test at FNAL

FPIX2 (8 µm pixel) x 4
SOFIST_v1 (20 µm pixel) x 2

σ = 1.14 µm
σ = 0.87 µm
σ = 1.00 µm
σ = 3.9 µm
The position resolution of FPIX2 demonstrated by MC

- Intrinsic position resolution is expected to be $\sim 0.7 \, \mu m$!
- No evaluation systematic error yet
- Tracking resolution is $\sim 0.5 \, \mu m$
Stitching Exposure for Large Sensor

Mask Layout

Exposed Layout
SOI Photon-Imaging Array Sensor (SOPHIAS) for X-ray Free Electron Laser (XFEL) SACLA

Utilization of SOPHIAS has been started for various experiments in SACLA@RIKEN.
• Dynamics of Atomic Structure
• Direct Observation of Chemical Reactions
• etc.

Dual Sensor Camera

X-ray Tube Cu 22kV 400uA
5000 frames accumulated
(total exposure: 500 s)
Sensor-detector: 2m
XRPIX: Event Driven X-ray Astronomy Detector

- Chip size: 24.6 mm x 15.3 mm
- Pixel size: 36 µm sq.
- # of pixel: 608 x 384 (= ~233k)
- Thickness of sensor layer: 310 µm (CZ wafer)
  500 µm (FZ wafer)

-55Fe
-60 °C, 100V
Single Pixel

Counts

Energy (keV)

55Fe
FWHM: 3.2% (190 eV)

10 e⁻ (rms)
IV. Summary

• SOI pixel technology becomes mature. Back-gate and sensor-circuit coupling issues are solved by introducing double SOI wafer.

• Radiation tolerance is improved to more than 10 Mrad by biasing middle Si of the Double SOI.

• NMOS-PMOS active merge reduces layout size very much. This is almost equivalent to go to finer process while keeping analog voltage of 0.2um process (1.8V/3.3V).

• Many kinds of SOI X-ray detectors are developed (or under development) so far.

• Our SOI Pixel process run is open to academic people. Please join the run.
11th International “Hiroshima” Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD11) in conjunction with 2nd Workshop on SOI Pixel Detector (SOIPIX2017)


TOPICS:
- Simulations
- Technologies
- Pixel and Strip Sensors
- Radiation Tolerant Materials
- ASICs
- Large Scale Applications
- Applications in Biology, Astrophysics, Medical, ...
- New Ideas and Future Applications
- SOI Detectors

KEY DATES:
- Abstract submission: 10 July - 28 Aug.
- Registration: 10 July – 20 Nov.

https://indico.cern.ch/event/577879/

For further information – email: hstd@ml.post.kek.jp