ID de Contribution: **47** Type: **Non spécifié**

Studies on radiation-hardness of CMOS integrated circuits for Phase I and Phase II LHCb Upgrades

mardi 15 octobre 2019 18:35 (5 minutes)

The read-out electronics for complex particle detectors need to meet technological constraints such as operating at top performance and high-speed in environments with hard radiation: hard hadrons spectra and very large Total Ionization Dose (TID). Being exposed to a harsh mixt-radiation field, the semiconductor devices must defy progressive degradation and susceptibility to singular failures. In support for Phase I of Large Hadron Collider beauty (LHCb) detector Upgrade Program, the LHCb Romanian Group has contributed to the radiation hardness qualification tests, data analysis and extrapolation for CMOS integrated circuits. ASICs like MAROC3 and SPACIROC2 produced by Omega Laboratory were tested. Commercial solutions like the FPGA integrated circuits - KINTEX-7 from Xilinx and the Axcelerator antifuse FPGA from Microsemi were tested, too. Radiation-induced effects dependent on the total ionizing dose (TID) have been measured and investigated. The Single-Event Effects (SEE) observed in the integrated circuits were counted and classified, and the relevant cross-sections of SEE calculated. Some mitigation methods were implemented and the efficiency to lower the SEE rate was quantified.
This report summarizes the Bucharest-group work done over five year in collaboration with LHCb and other international partners, and the experiments done at several international facilities where various beams of particles were used to qualify the CMOS integrated circuits.
We report the TID effects and thresholds in ASICs, the operational efficiency degradation at very high TID rates above 10 rad/s, the very fast room-temperature annealing process which was parametrized and recovers completely the device within the initial operational parameters.
Further, the reliability of KINTEX-7 FPGA was tested up to 1 Mrad (Si) and for antifuse FPGA up to 8 Mrad(Si) without any sign of permanent effects. An analytical model is developed for leakage current parametrisation at high TID rate, and is used to extrapolate to the LHCb environment for 50 fb-1 and beyond.
The KINTEX-7 FPGA was subject to an extensive ion SEE testing campaign for estimating the effects on operation of 3000 FPGAs in the Phase I of the LHCb Upgrade. We estimate a rate of 20000-30000 Single Event Upsets (SEUs) per hour in 3000 FPGAs, each with 19 Mb configuration memory. In total there are about 60 SEUs per hour critical failures. High current events ca be triggered by a very small fraction of SEU occurring in FPGAs configuration memory and by Single Event Latch-Ups (SEL). Online partial/full reconfiguration will be used as error mitigation for Upsets and power cycles of FPGA boards for SEL. The anti-fuse FPGA were tested in conditions similar to what is expected for LHCb Phase II Upgrade during HL-LHC runs.

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Classification de Session: Poster session