Suivi de projet du SERDI

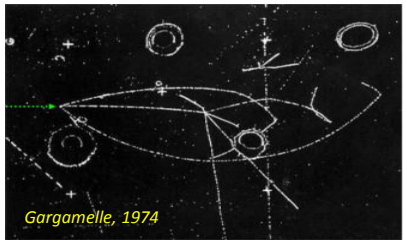
« **ATLAS** (**A** **T**oroidal **L**arge Hadron Collider **A**pparatu**S**) »

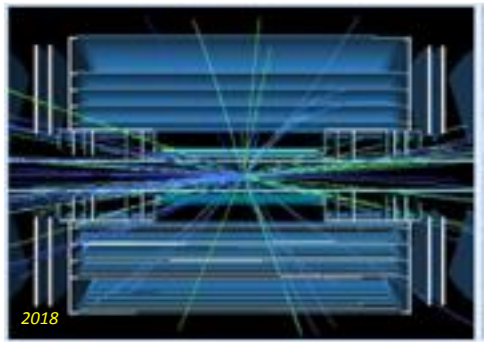
(Détecteur, Instrument, Dispositif)

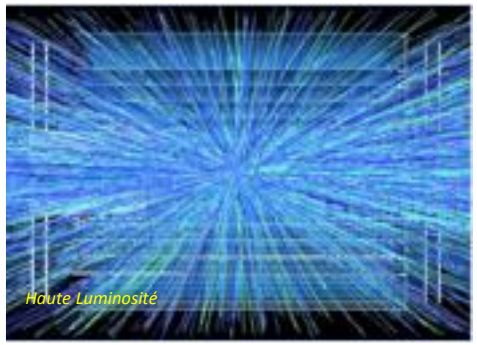
Maurice Cohen-Solal,
Jimmy Jeglot, Olivier Lemaire,
Jihane Maalmi, Jean-Luc Socha,
Christophe Sylvia, Philippe Vallerand.

(SERDI - LAL – Université Paris-Saclay)

(3 stagiaires *ESIEE*)







LHC interaction

Membre de la « « Collaboration RD53» »

RD 53 Collaboration :

Development of pixel readout integrated circuits for extreme rate and radiation

RD53 Working Group

- **WG1** : Radiation (*Marlon Barbero*)
- **WG2** : Top Level Design (**Maurice Garcia-Sciveres**)
- **WG3** : Simulation Test Bench (Tomasz Hemperek)
- **WG4** : I/O (Roberto Beccherle)
- **WG5** : Analog Design (Valerio Re)
- **WG6** : IP Blocks (Jorgen Christiansen)

Flavio Lodo : integration (micro électronique)

RD53 3 Weekly Vydio meetings and physical meetings on test and design

ITk-LAL Weekly physical meetings on Itk project

ITk-France Weekly vydio meetings and physical meetings on module

RD50 - Radiation hard semiconductor devices for very high luminosity colliders

~150 people from ~ 30 institutes :

- Bonn University
- CERN
- Dortmund
- Fermilab
- University of Glasgow
- INFN : Bari - Bergamo-Pavia - Milano - Padova - Perugia - Pisa - Torino
- IN2P3 : **CPPM** - LAL - LAPP - **LPNHE**
- **LBNL**
- New Mexico
- NIKHEF
- Prague IP/FNSPE-CTU
- RAL
- Seville University

Groupe de physique :
Abdénour Lounis, *Vasyl Drozd, Tasneem Rashid*, Dymitris Varouchas, Kostiantyn Sakhatskyi, Dmytro Hohov, Marc Escalier, Anatolii Korol, Anastasia Kotsoechagia.

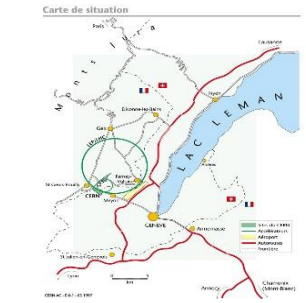
Mécanique : Aboud Fallou.

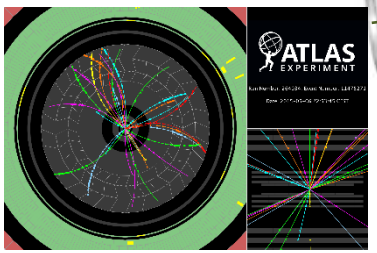
Instrumentation : Stéphane Trochet.

Mission : *D. Breton*

Pôle : *M. El Berni*

« ATLAS »





Calorimétrie à tuiles

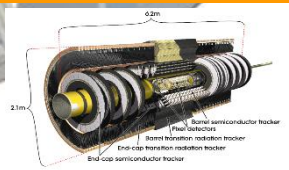
Argon Calorimeter

Remplacement de l'électronique de lecture

Spectromètre à muons

protons

Détecteur interne

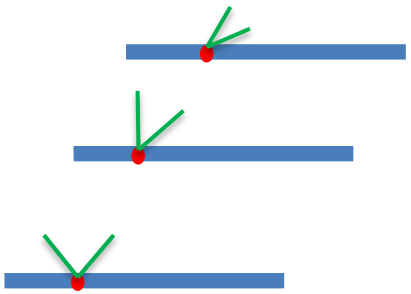


Upgrade Project

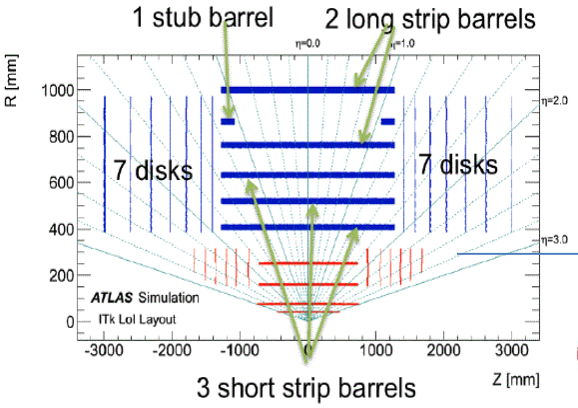
Remplacement intégral

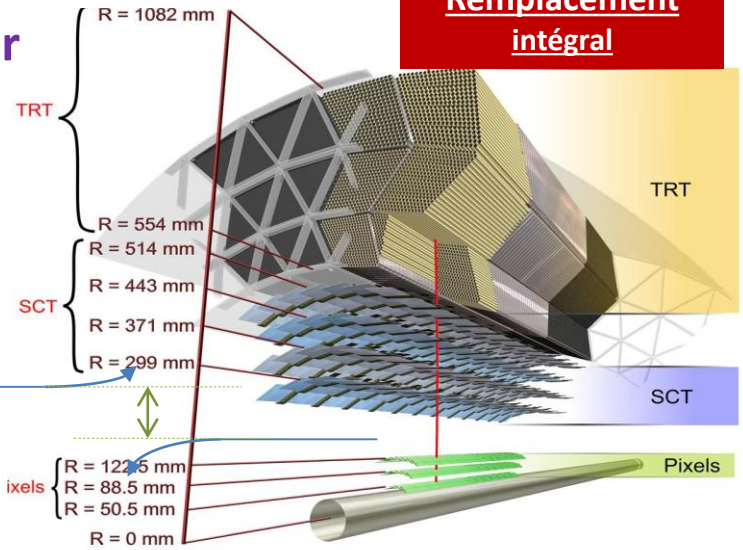
- Localiser les vertex (3 dimensions)
- Haute résolution en r.φ (50µm)
- Paramètres d'impact (15 µm)

détecteur de positions → tracking

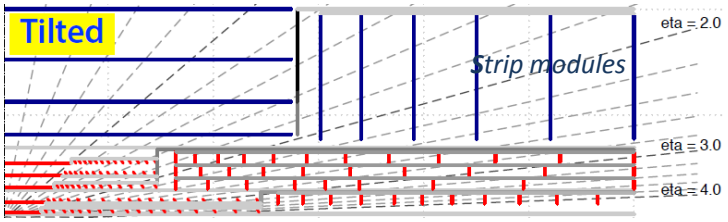


Tracker





« Objectifs »



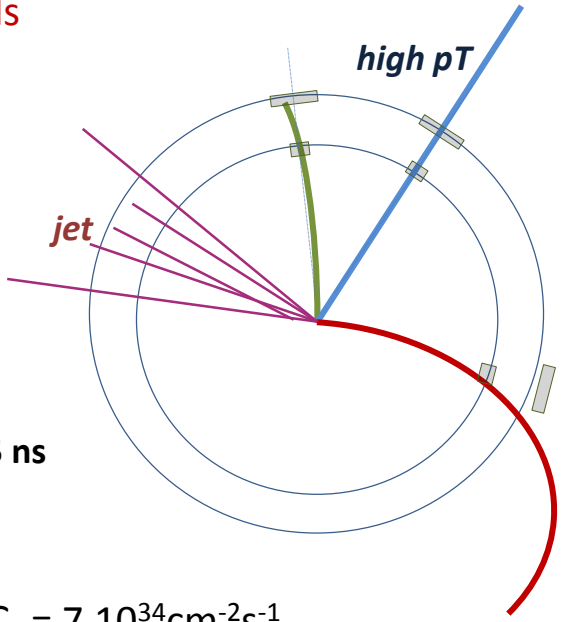
5 couches de pixels

90 363 520
voies de mesure

~ 180 m²
pixel

Centre de mass = 14 TeV

Fréquence collision 40 MHz ≡ **25 ns**



Luminosité = 7x LHC = HL-LHC = $7.10^{34}cm^{-2}s^{-1}$
10^{11} protons par paquet

~ **200 événements** (interactions) par Beam Cross

(actuellement 24)

Radiation 10MGy = 1 (à 2) **GRad**

$1.5.10^{15}$ n_{eq}/cm^2 sur 10 ans

(actuellement 200MRad)

=> Haute granularité

Technologie TSMC **65 nm** CMOS

(actuellement 130 nm)

50 µm x 50 µm (actuellement 50x 250)

Puce ~ 20 mm x 20 mm (~10^9 transistors)

400 colonnes x 400 lignes
(actuellement 80)

Soit 160 000 voies d'électronique par puce

(actuellement 26 880)

Hit ~ 2(3) **[GHz / cm²]**

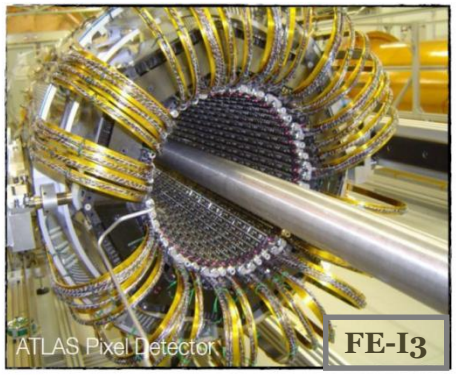
(actuellement 10 fois moins)

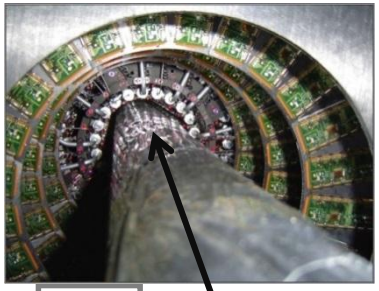
Hit ~ 500 [MHz /cm²] (taux de traces constantes)

L1 Latence ~ 12.8 µs (actuellement 3µs)

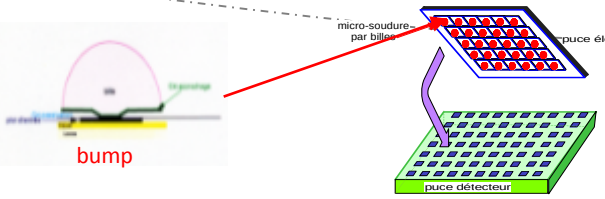
Débit : 4 (5) Gb /s /chip

Features of electronics chips

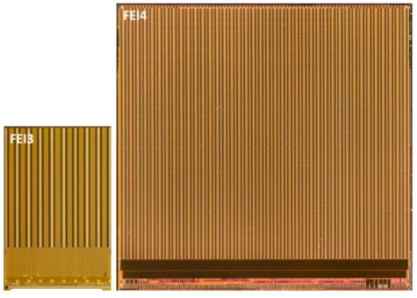




Insertable B-Layer

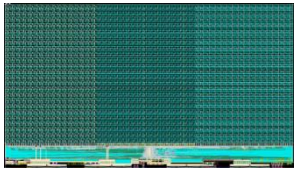


5 ATLAS pixel institutes



FEI3 FEI4B

7 ATLAS pixel institutes



RD53A

30 ATLAS pixel institu

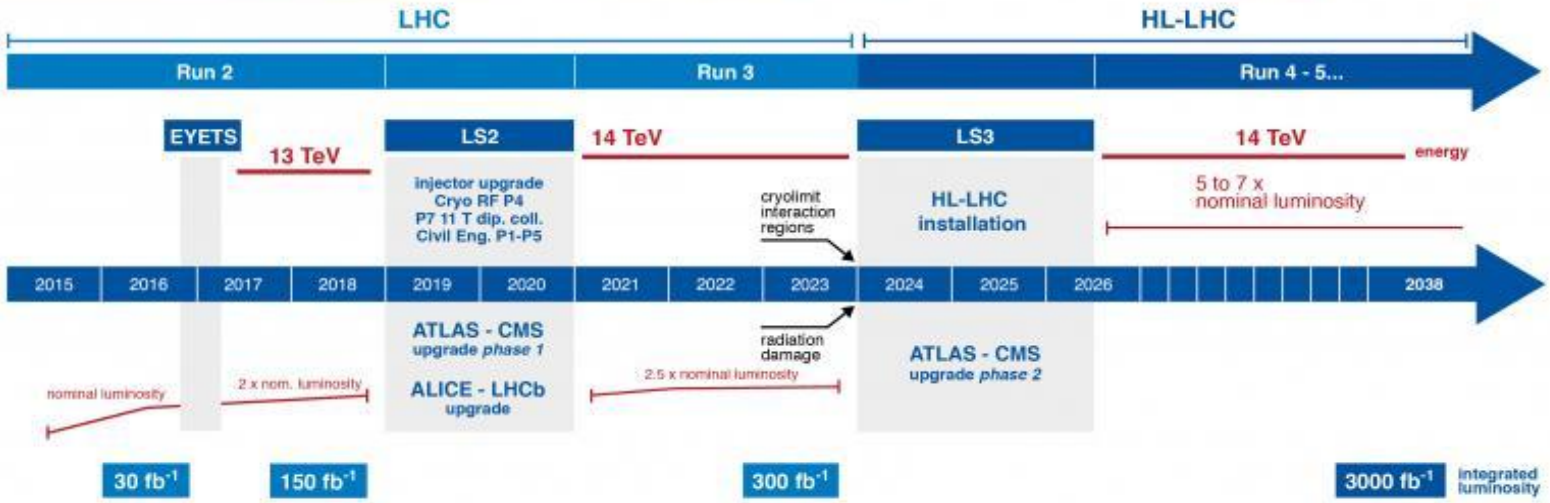
ATLAS-ITk

Biggest chip in HEP to date

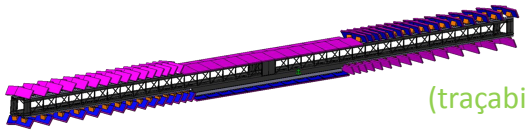
LHC-HL *(2023)* :

	500 k€	2 M€		
	FEI3	**FEI4B**	**RD53A**	**ATLAS**
Année	2003	2011	**2017**	2019 ?
Technologie [nm]	250	130	65	65
Taille [mm²]	7.6x10.8	20x19	20x11.8	20x21
Zone active [%]	74	89	81	91
Array	160 x 18	400 X 80	192 x 400	384 x 400
Nombre de pixel	2 880	26 880	76 800	153 600
Taille pixel [µm²]	**50 X 400**	**50 X 250**	**50 X 50**	**50 X 50**
Nombre de transistors [Million]	3.5	87	550	940
Débit de sortie [Gbit/sec]	0.04	0.64	2 x 1.28 & ~~5.12~~	Idem ?
Rendement [%]	80	60	?	?
Puissance [W/cm²]	0.25	0.25	0.5	1

« Planning »



Démonstrateur ITk (2018 – en cours)



(traçabilité)

Production des sensors : 2020

RD53A (Q4-2017)

Début production des modules 2022

Test caractérisation RD53A (Q4-2017 – Q2-2019)

Installation ITk (Q4- 2023)

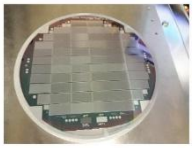
FE ATLAS Design (Avril 2019)

« Upgrad» (Q1-2025)

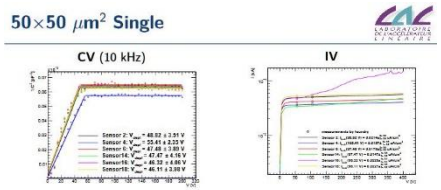
FE ATLAS soumissions (Juin 2019)

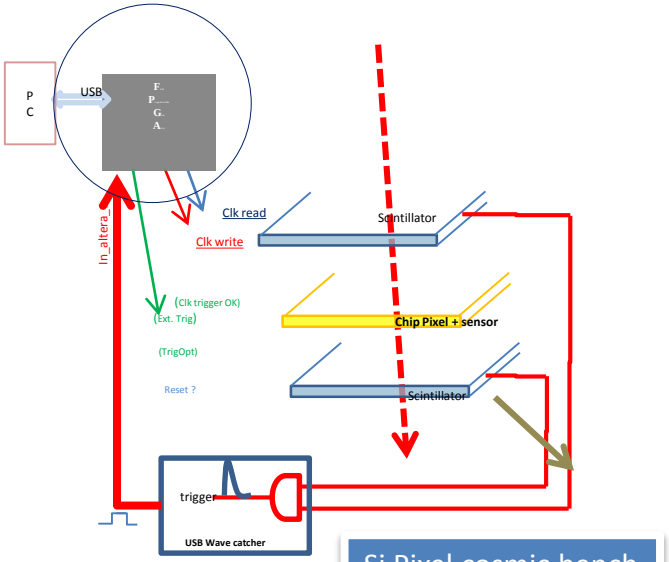
Commande des tranches : sept. 2020

Caractérisation Sensor + RD53A au LAL



Sensor Épaisseur
150 µm



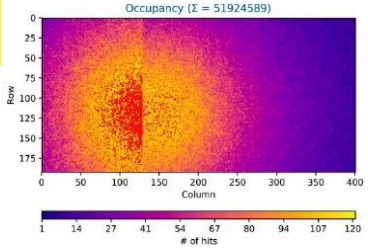


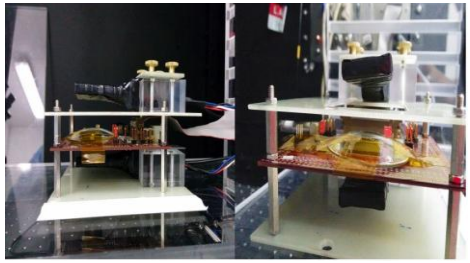
Si Pixel cosmic bench

Laser Testing Station

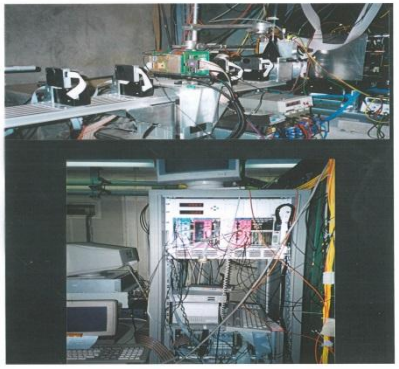
Source Scan with BDAQ53

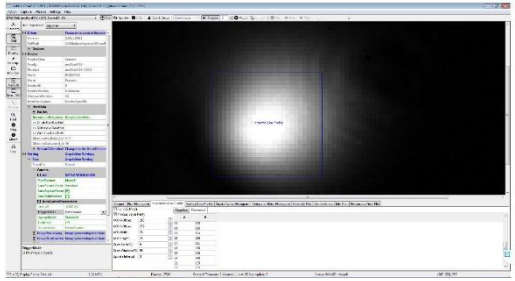
RD53A





BEAM
TELESCOPE





Beam Shape

Configuration 1/2 Column of 200 Cells

Cells folded

14 x 14 + 4 cells **chained** (« snake »)

2 shift registers

13	14	41	42	69	70	97	98	125	126	153	154	181	182
12	15	40	43	68	71	96	99	124	127	152	155	180	183
11	16	39	44	67	72	95	100	123	128	151	156	179	184
10	17	38	45	66	73	94	101	122	129	150	157	178	185
9	18	37	46	65	74	93	102	121	130	149	158	177	186
8	19	36	47	64	75	92	103	120	131	148	159	176	187
7	20	35	48	63	76	91	104	119	132	147	160	175	188
6	21	34	49	62	77	90	105	118	133	146	161	174	189
5	22	33	50	61	78	89	106	117	134	145	162	173	190
4	23	32	51	60	79	88	107	116	135	144	163	172	191
3	24	31	52	59	80	87	108	115	136	143	164	171	192
2	25	30	53	58	81	86	109	114	137	142	165	170	193
1	26	29	54	57	82	85	110	113	138	141	166	169	194
0	27	**28**	55	**56**	83	**84**	111	**112**	139	**140**	167	**168**	195
													196
													197
													198
													199

srin_A
srin_B

Clk_A
Clk_B

Sel_(A or B)

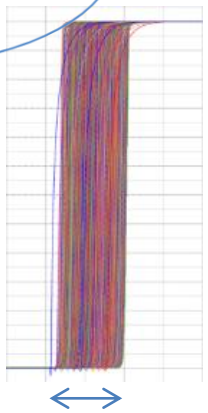
SR_Out_Low

SR_Out_High

Configurations des pixels
12 bits / pixel

Skew simulation < 1nsec
(between 400 cells)

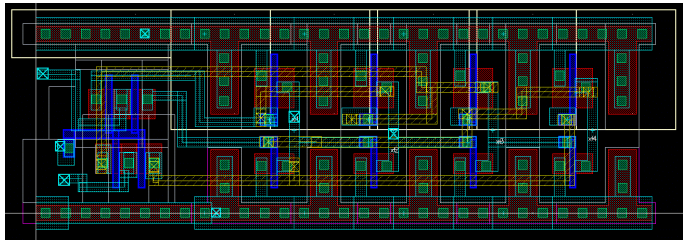
Buffers (repeater) each 40 cells
and inside the pixels



CPPM latch « normal »

CPPM Latch « enclosed »

50µm * 400 = 20 mm lines
(8 pF)

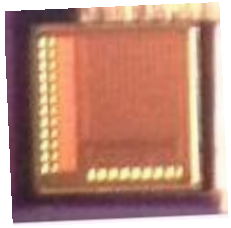


One new design Dice radhard latch

Conf Column Chip (C3)

Layout « top level »

TSMC 65nm



- Size **1 mm x 1 mm**
  (pitch 50µm x 50µm)
- PADs on 2 sides

200 “pixels”

≡ ½ column

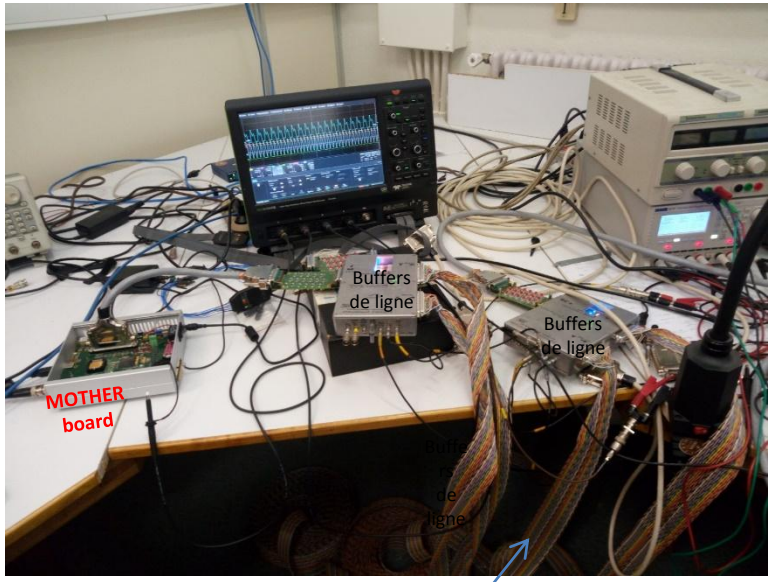
SPI

Logic Interface

Output mux

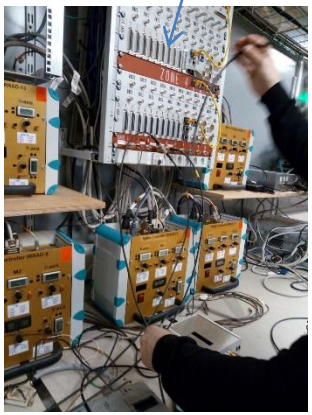
Back on july 16

Setup Test board C3 at LAL & at CERN



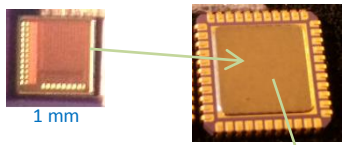
30 mètres de
câbles

Patch panel



installation

C3
1 mm
1 mm

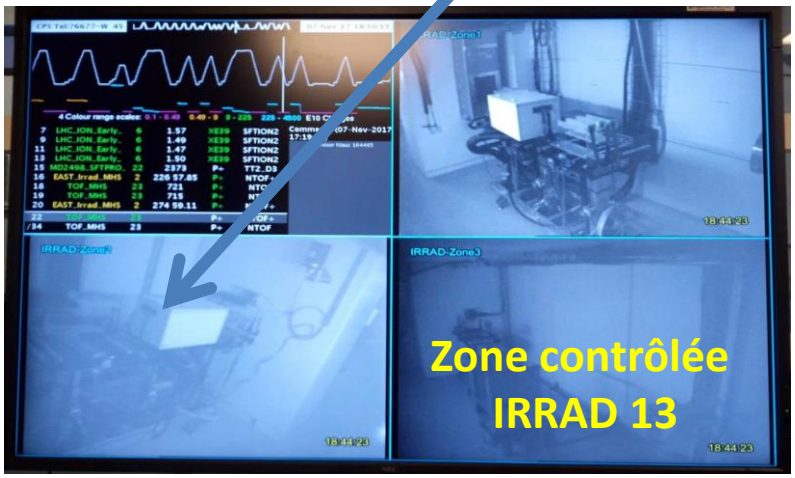


Mezzanine
board V2

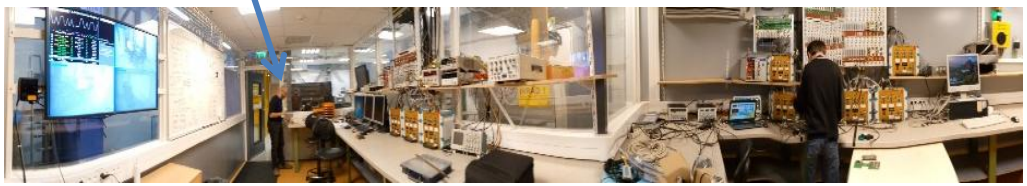
FPGA

Vers la boite buffer

MOTHER board
V2

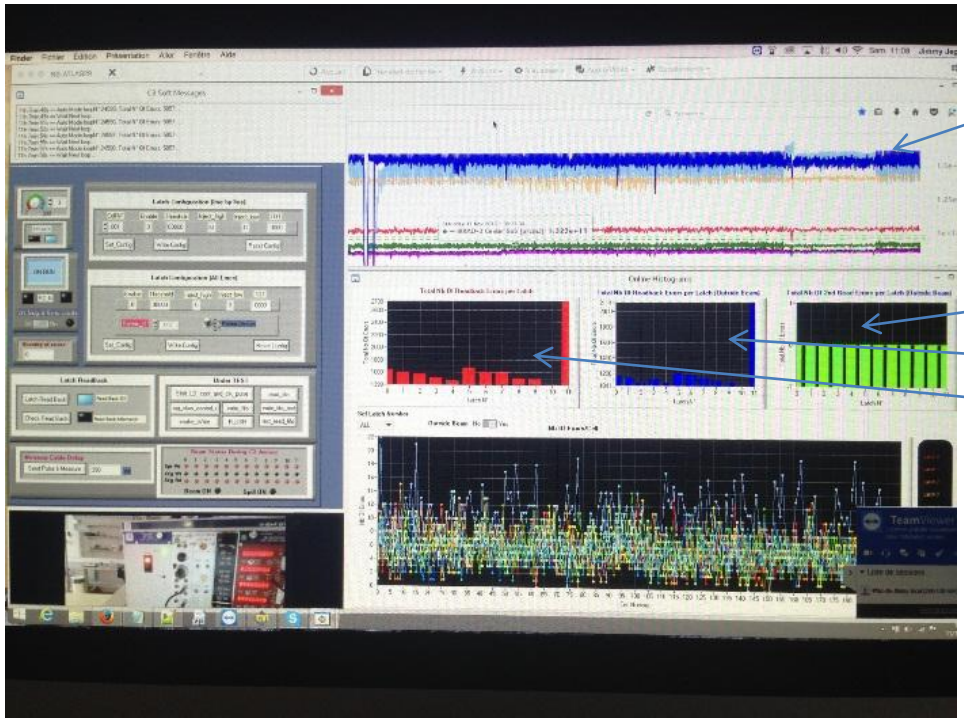


Fédérico
(cern)



(Maurice, Jimmy, Christophe, Dominique, Mowafak)

Fonctionnement normal en irradiation



Proton energy: **24 GeV**

Flux 3e^8 protons/cm2

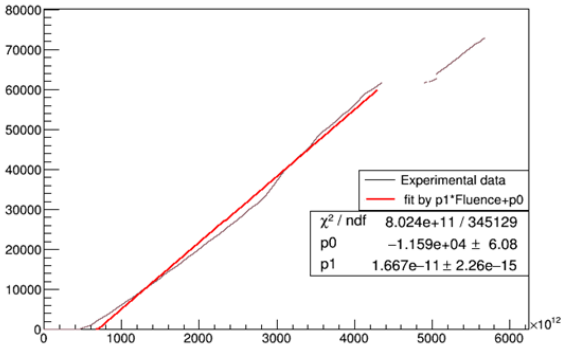
Erreurs RadHard latches :

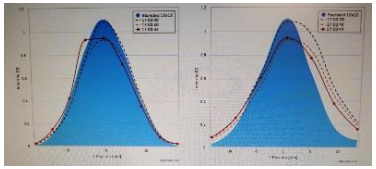
Dose intégrée

Singe Event Upset

Singe Event Upset
(pendant le faisceau)

Single Event Upset intégrés





Positions transverse

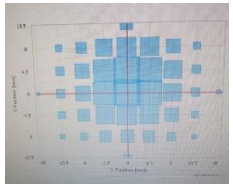
Sections efficaces mesurées :

$$\sigma_{\substack{standart \\ flip-flop}} \approx 2.8 \times 10^{-14} cm^{-2}$$

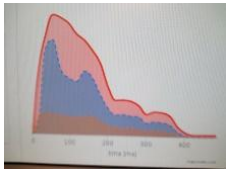
$$\sigma_{normal} \approx 6.2 \times 10^{-15} \mathrm{cm}^{-2}$$

$$\sigma_{enclosed} \approx 5 \times 10^{-15} \mathrm{cm}^{-2}$$

$$500\ [MHz/cm^2] \times 160\ 000\ \times 16 \times 2.8e^{-14}\ = 64\ bits\ flips\ [sec^{-1}]\ par\ chip\ pixel$$



Profil transverse
(5mm x 5mm)



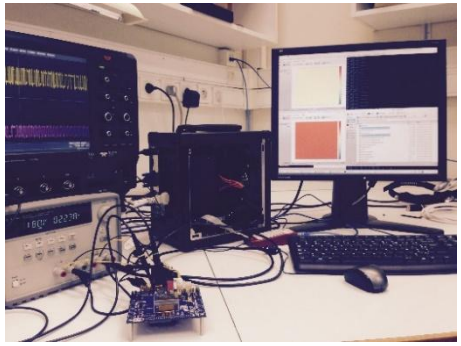
Profil longitudinal

1% des pixels affectés après 48 [*sec*]

(Jimmy, Jihane, Christophe, Kostantin, Maurice)

RD53A Yarr, BDAQ53 & Laser system at LAL

- **YARR**



Xpressk7 board
+ Fmc Ohio

mini Display
Port cable

- Xpressk7 k325
- FMC Ohio board
- **Mini display port RD53A - SCC**
- **CentOS**

https://gitlab.cern.ch/

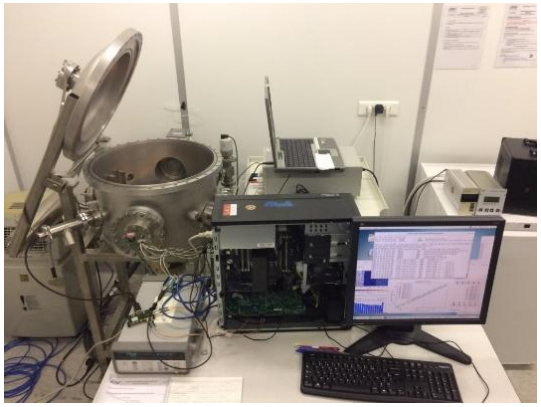
- **BDAQ53**

KC705

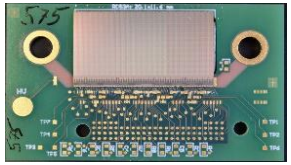
- Mini display port - SMA

ASUS H1 10I-
PLUS computer

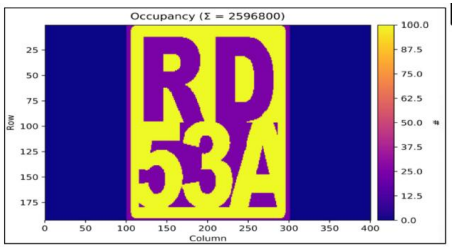
4 mini Display Port on
Ohio Fmc board

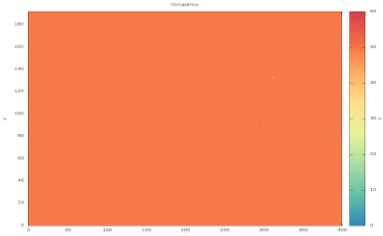


Enceinte thermique

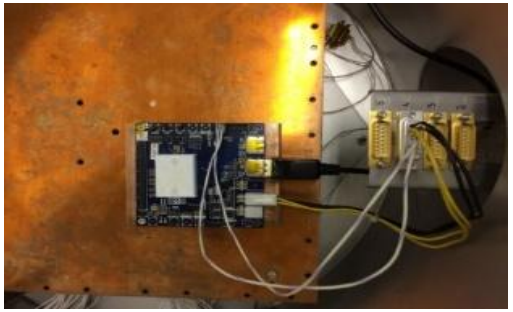


RD53A
Arrivé Décembre 2017





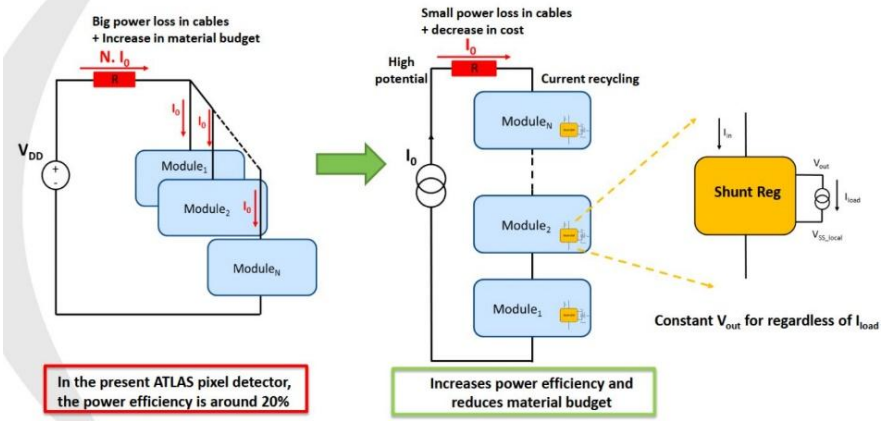
rd53a_proto_analog_Occupancy__LDO

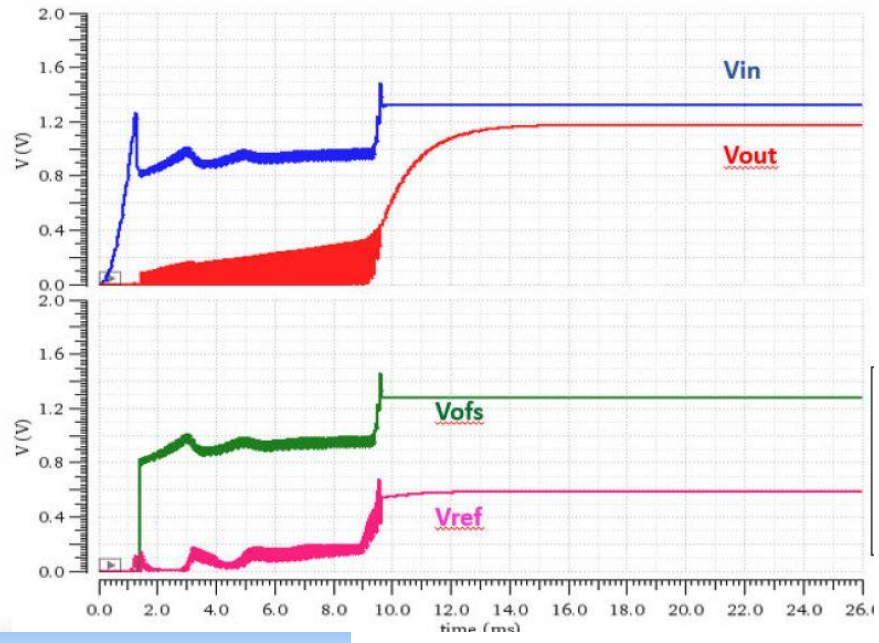


(Jimmy)

Simulation Shunt Low Drop Out au LAL

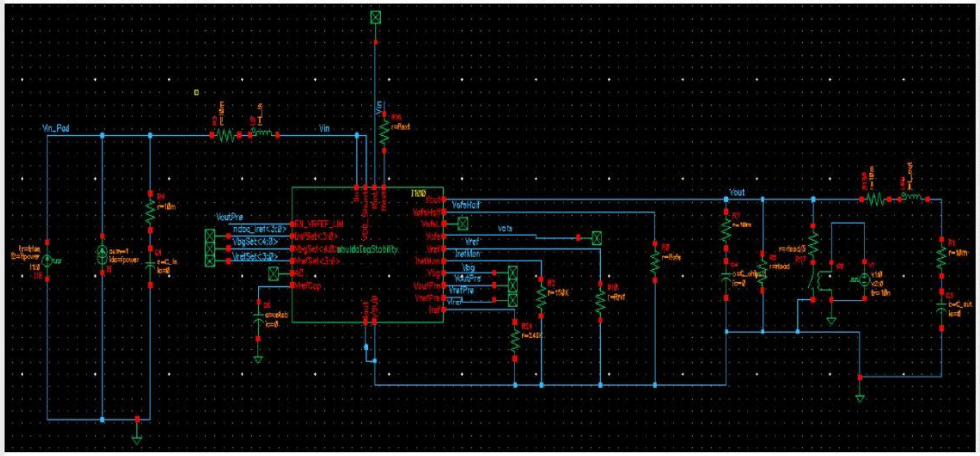
Serial powering in new ATLAS pixels





ShuntLDO simulation – firsts studies

Circuit scheme and its parameters studding



Design Variables

	Name	Value
1	VbgSet	25
2	VrefSet	8
3	C_chip_d	300n
4	C_in	6u
5	C_out	2.2u
6	ndac_iref	8
7	cstab	1n
8	ipower	0
9	itpower	1
10	L_in	1n
11	L_out	1n
12	Rext	600
13	rload	1K
14	Rofs	125K
15	Rref	150K
16	trise	5m

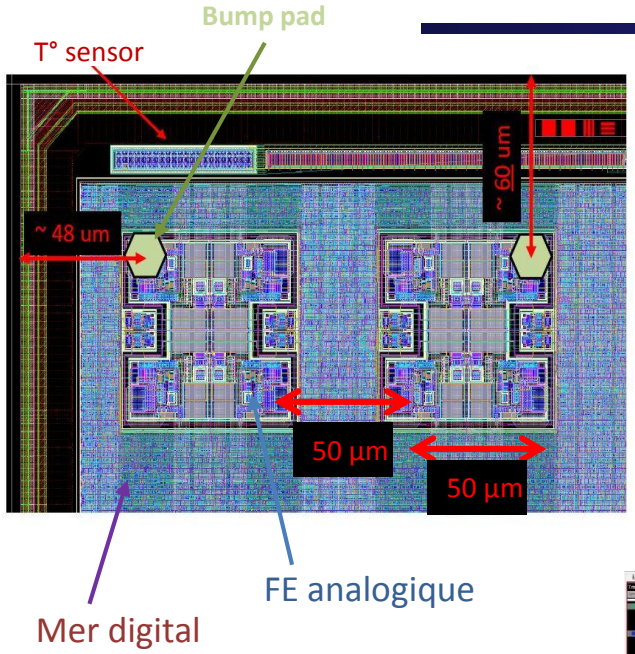
SERDI
Service d'Electronique, Recherche en Détecteurs et Instrumentation

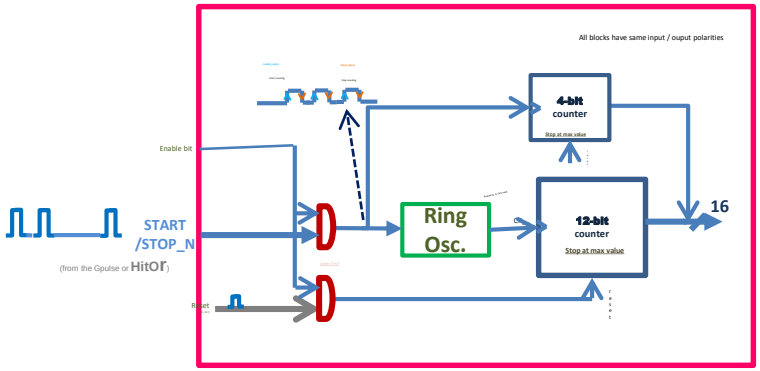
LAL
LABORATOIRE DE L'ACCÉLÉRATEUR LINÉAIRE

(Kostantin, C. Sylvia, P. Vallerand)

RD53A & Ring oscillator block diagram & layout

TSMC 65nm technology





Moniteur d'irradiation

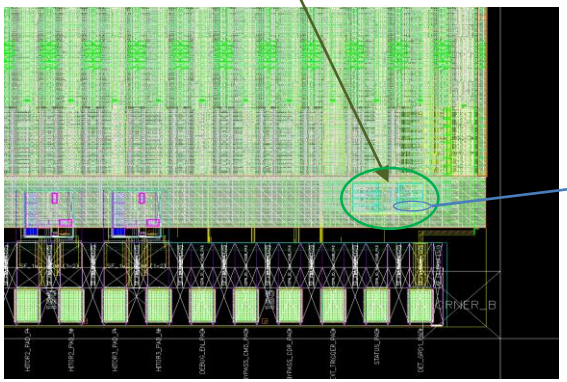
Seuils , TOT, …

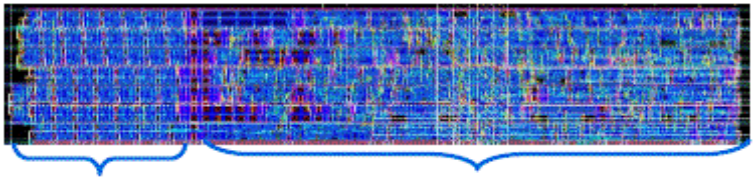
TOT haute résolution

8 similar ring oscillators with **cells :**

INVD0, INVD4, NDD0, NDD4, NRD0, NRD4, CKND0, CKND4

8 oscillators placed in bottom right corner of RD53A





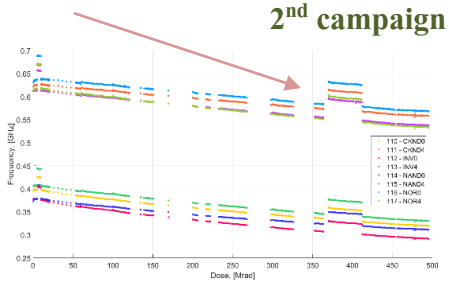
Typical oscillator

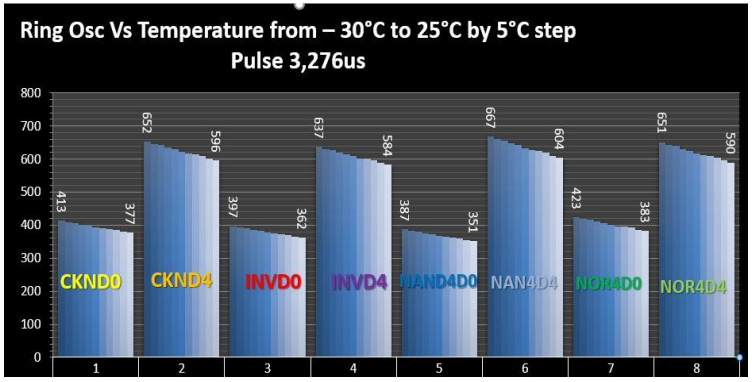
RD53A T° & X ray measurements

- With excluding of the data for periods, when ***Vddd*** jumped.
- (Cutting: ***Vddd > 1.13V & Vddd < 1.15V***)

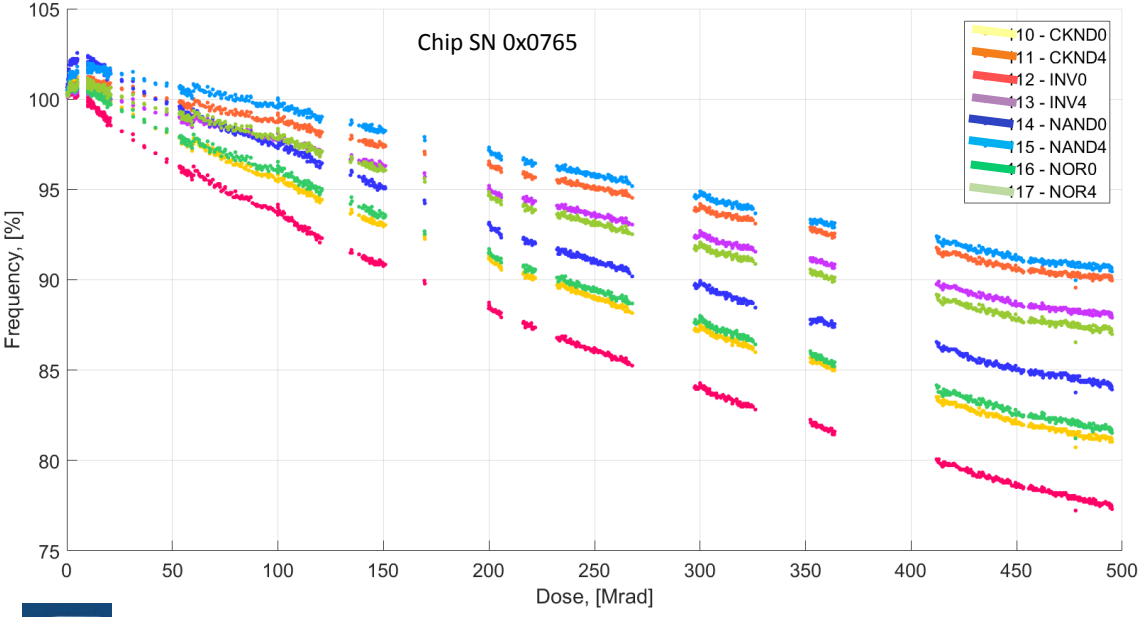
2nd campaign at CERN

(August 2018)

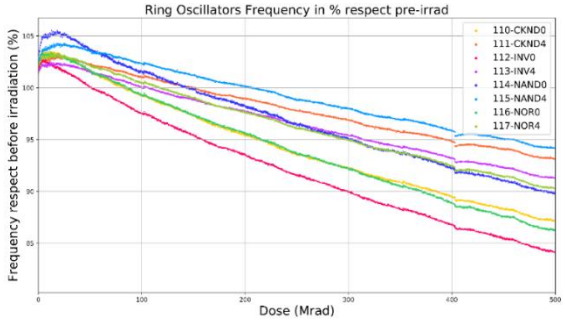




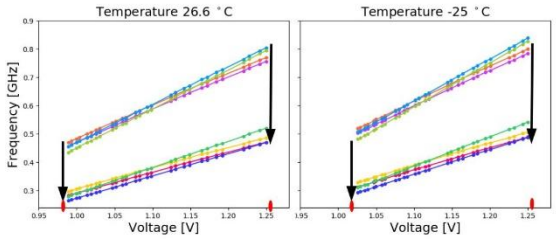
RD53A



LAL measurements

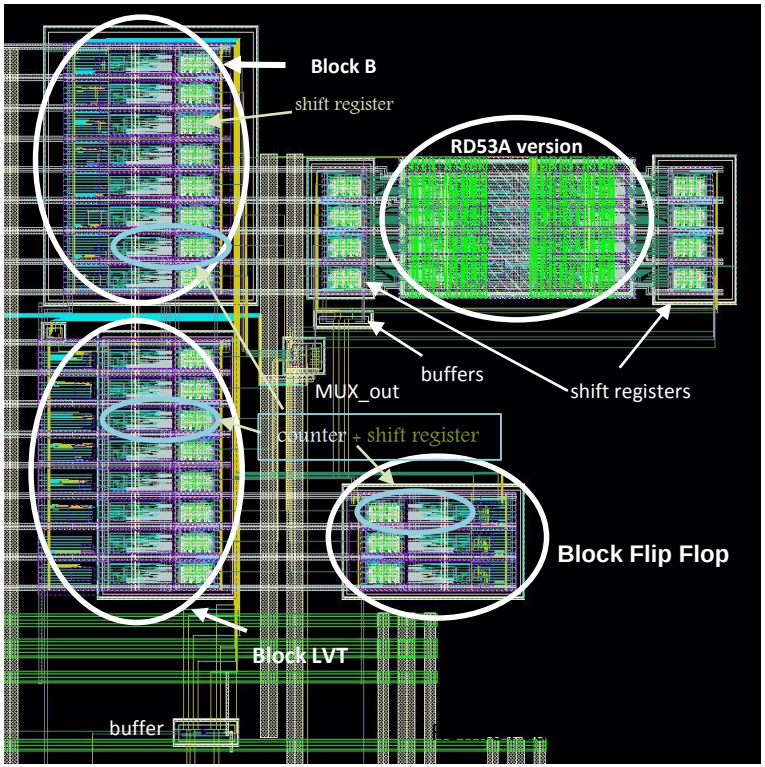


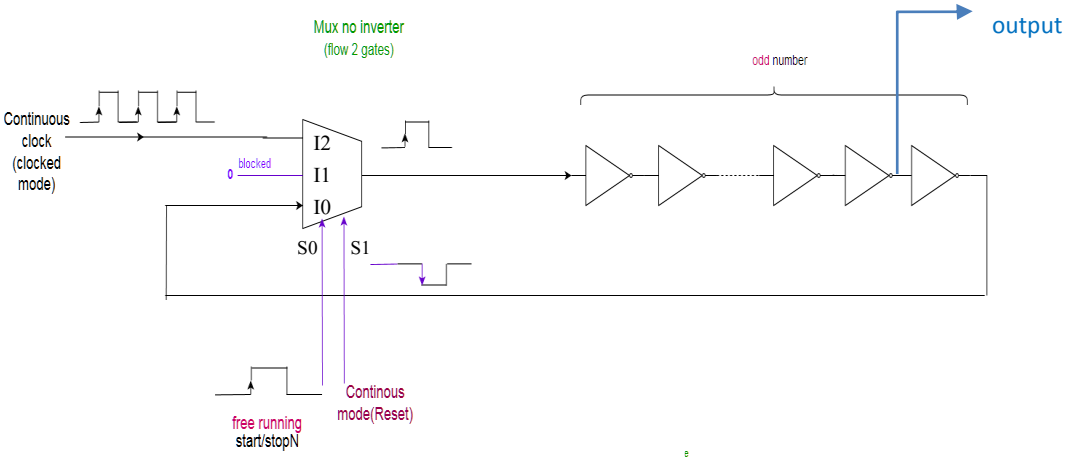
Glasgow measurements



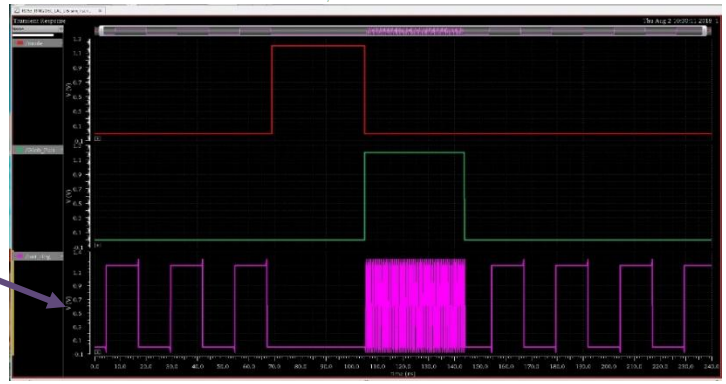
(Vasyl Drozd, Luis Miguel Casas, Dzmitry Maneuski, Jimmy Jeglot, Maurice Cohen, Anatolli)

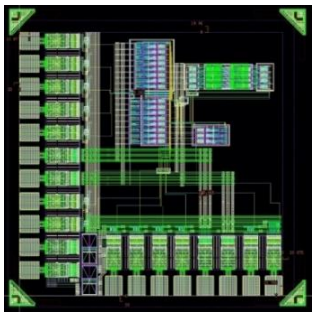
Ring Oscillators Monitor Integrated Circuit (ROMIC)





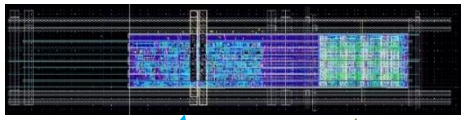
Ring oscillator output (clocked, blocked & free-run)

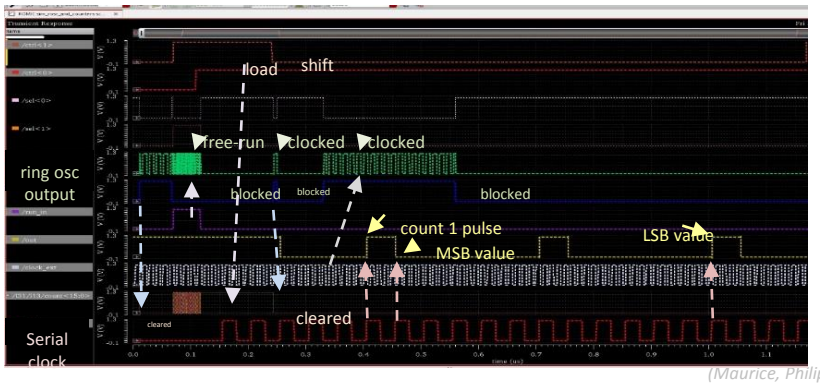




Submitted on November 12th, 18

LAL-ATLAS budget

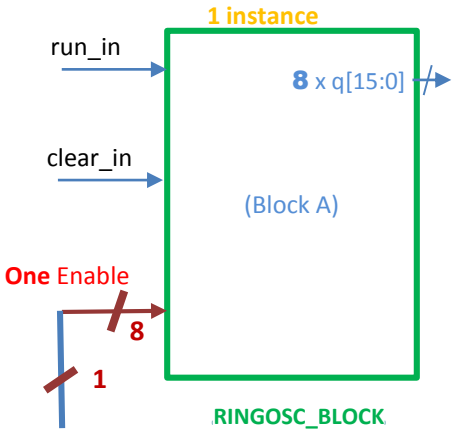




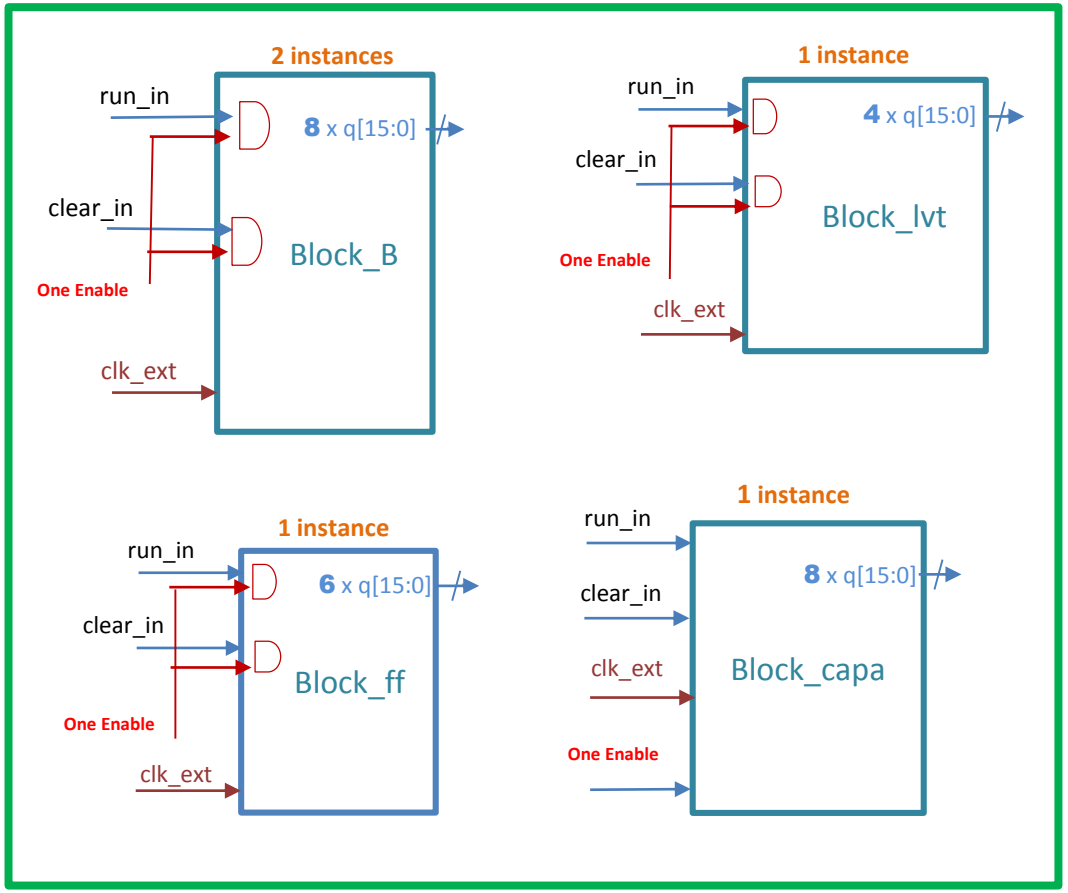
(Maurice, Philippe)

Ring Oscillator layout organisation in ATLAS CHIP

RINGOSC_BLOCK + RINGOSC_B

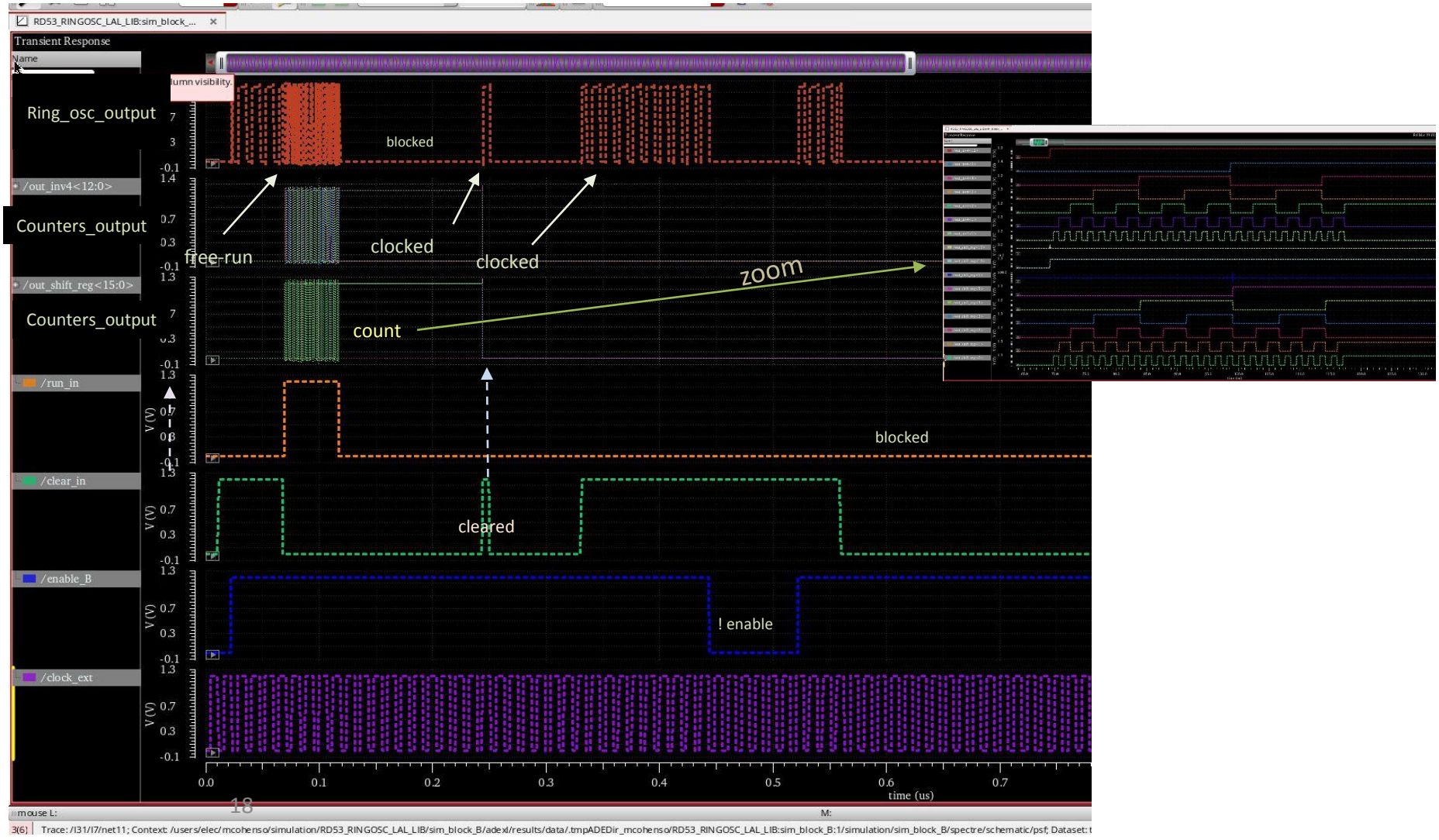


RINGOSC_B

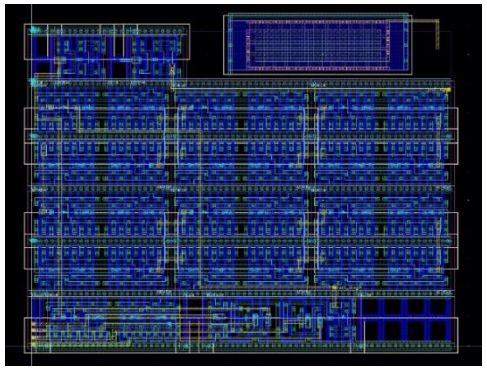


Total of (8+34) x 16 wires to routed !

RD53B Simulation [The whole block_B was simulated with Spectre]

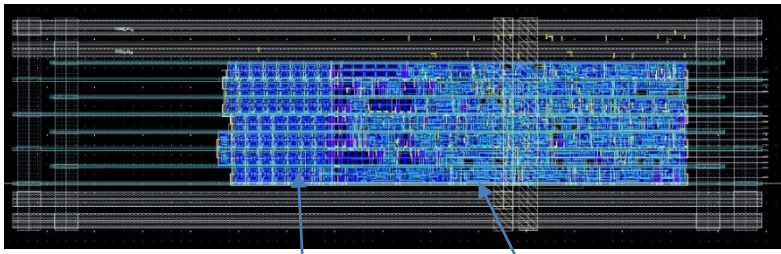


(Maurice c s, Kostiantyn Sakhatskyi)



One ring osc capacitance

Ring Osc + counters

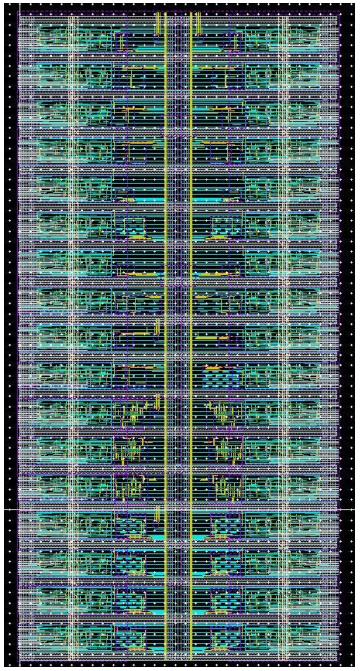


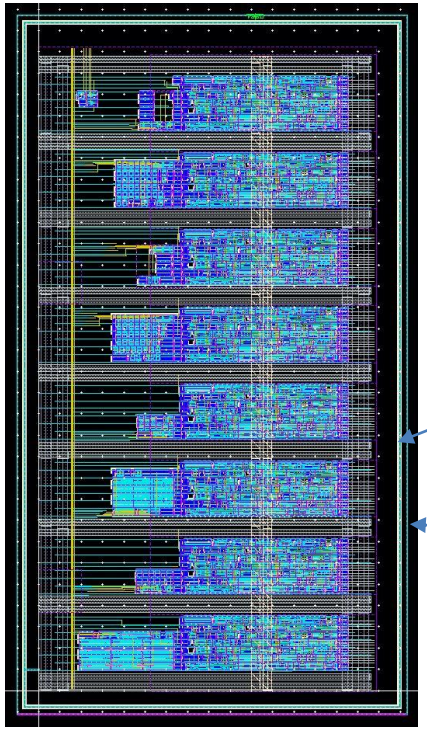
Virtuoso

Encounter Digital

Top cell incluant les 34 oscillateurs

(34 x 12 bits de sortie)





1 Block version B

guardring deep N well

guardring P substrate

Conclusion Need Help

All the symbols are finished but not all the schematics

Numerous simulations for all oscillators & blocks not yet finished :

- *extracted (room & -20°C)*
- *Slow corner (schematics, extracted , room & -20°C)*
- *Also versus VDD (schematics, extracted , scan T°)*

Blocks **simulations** (LVT, FF, Capa)

Layout :

A block ok
B block finished
FF (only ring osc)
LVT (only Ring Osc)

MOM Cap oscillator ongoing
(mesure de la dispersion de la capacité d'injection)

Top cell commencée

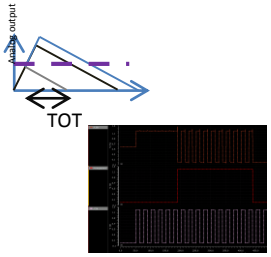
Abstract needed

Layout :

Verifications DRC, LVS (Calibre needed)

Modelling & specifications for RTL verification:

Verilog behaviour & Logic simulation to Verilog code



TOT haute resolution :

ROMIC chip is arrived (packaging ongoing)

ROMIC test, (card ok, firmware & software ongoing)

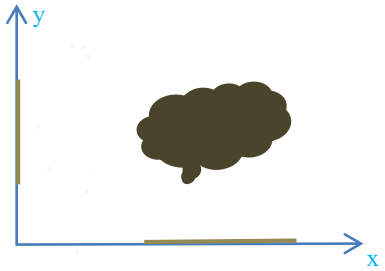
Final Design review
6-8 may at CERN

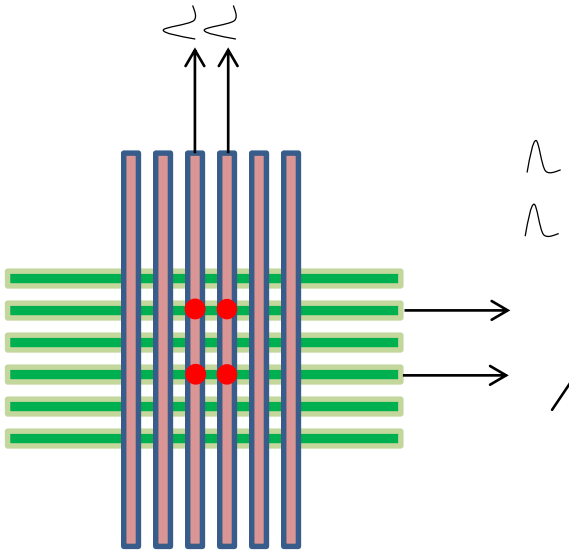
ROMIC could be used as stand alone chip in other applications

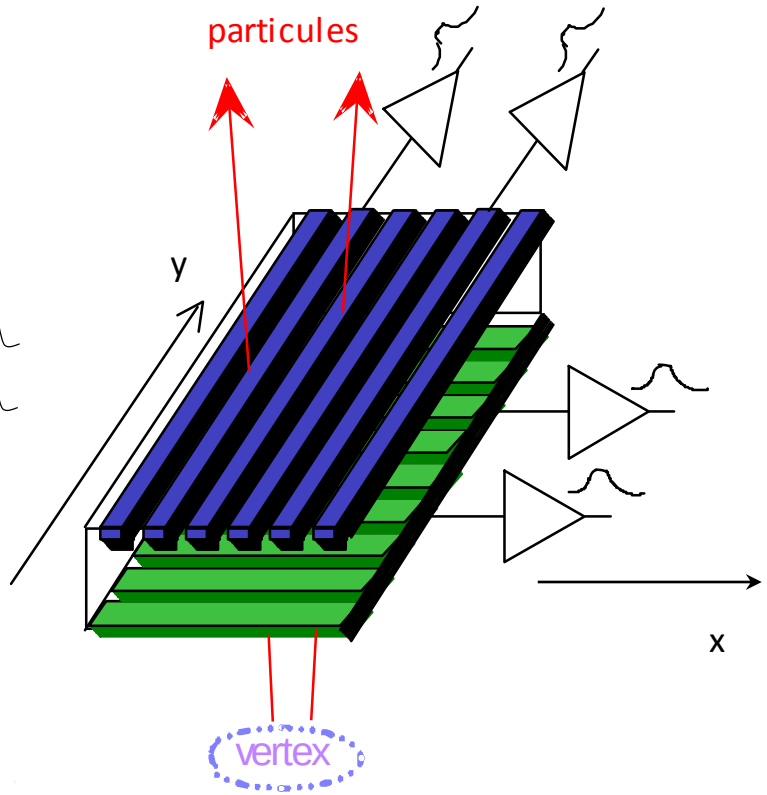
Backup slides

Pourquoi le développement des détecteurs pixels ?

- Micro-bandes (double faces)





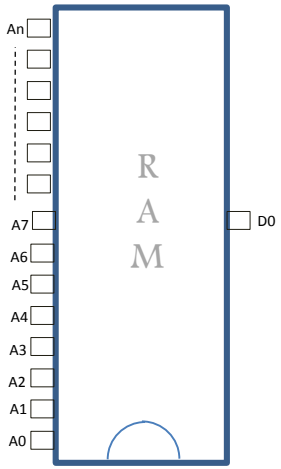


The silicon micropattern detector : a dream ?

(1987)

ABSTRACT

The present use of silicon microstrip detectors in elementary particle physics experiments is described and future needs are evaluated. Possibilities and problems to be encountered in the development of a true two-dimensional detector with intelligent data collection are discussed. This paper serves as an introduction to various other contributions to the conference proceedings, either dealing with futuristic device designs or with cautious steps on the road of technology development.



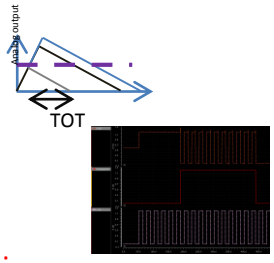
A faire (besoin d'aide)

All the symbols are finished but not all the schematics

Simulations of all RD53B oscillators:

- *Schematics & **extracted** (VDD, T°, verife the 40MHz)*
- *Same in Slow corner*
- *Add injection capacitance (dispersion)*

TOT haute resolution :



Climate chamber (in LDO & Direct powering):

- Exhaustive measurements (« absolute calibration »)
- Cross check with simulations
- Cross check Ring oscillators & CPPM sensors
- Digital scan
- Analog scan
- ….

Tests card for ROMIC (Firmware et Software)

ROMIC irradiation

Design the 5 oscillators flavours for RD53B
(in Deep N Well)

42 oscillateurs en tout

Modélisation comportementale

Mai – juin 2019 : intensives vérifications

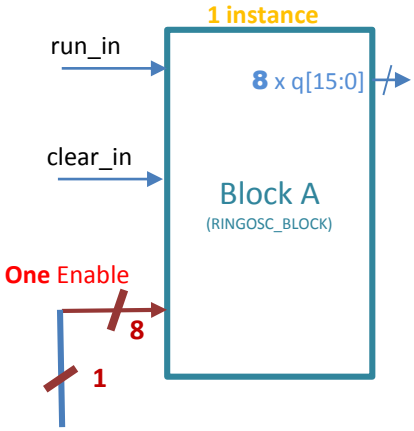
ROMIC could be used as stand alone chip in other applications

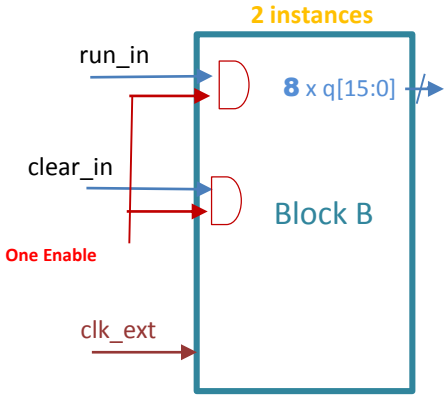
2 x RD53A assemblés bump bondé (LAL, LPNHE, avril 2019)

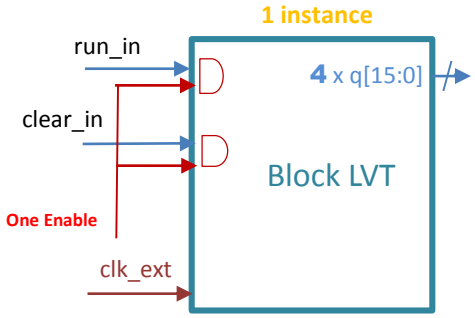
Intégration des modules (source, laser, faisceau)

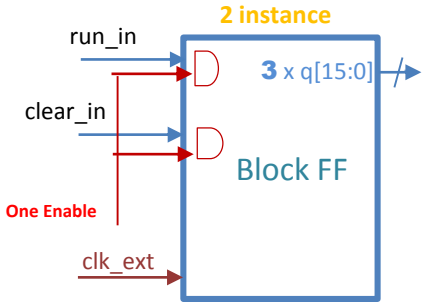
Septembre 2019 : arrivée de RD53B

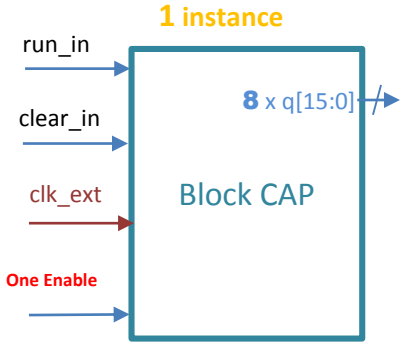
Power Service des modules ; stabilité.











Total of 42 x 16 wires to routed !

6 separated blocks
(**A, B, B, LVT, FF, FF, Capa**)

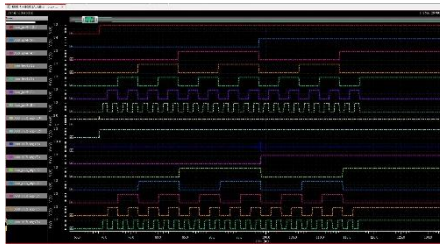
OR 1 BIG BLOCK ?

(Maurice Cohen, F. Lodo, Maurice Garcia)

RD53B Simulation *[The whole block_B was simulated with Spectre]*

counters zoom :

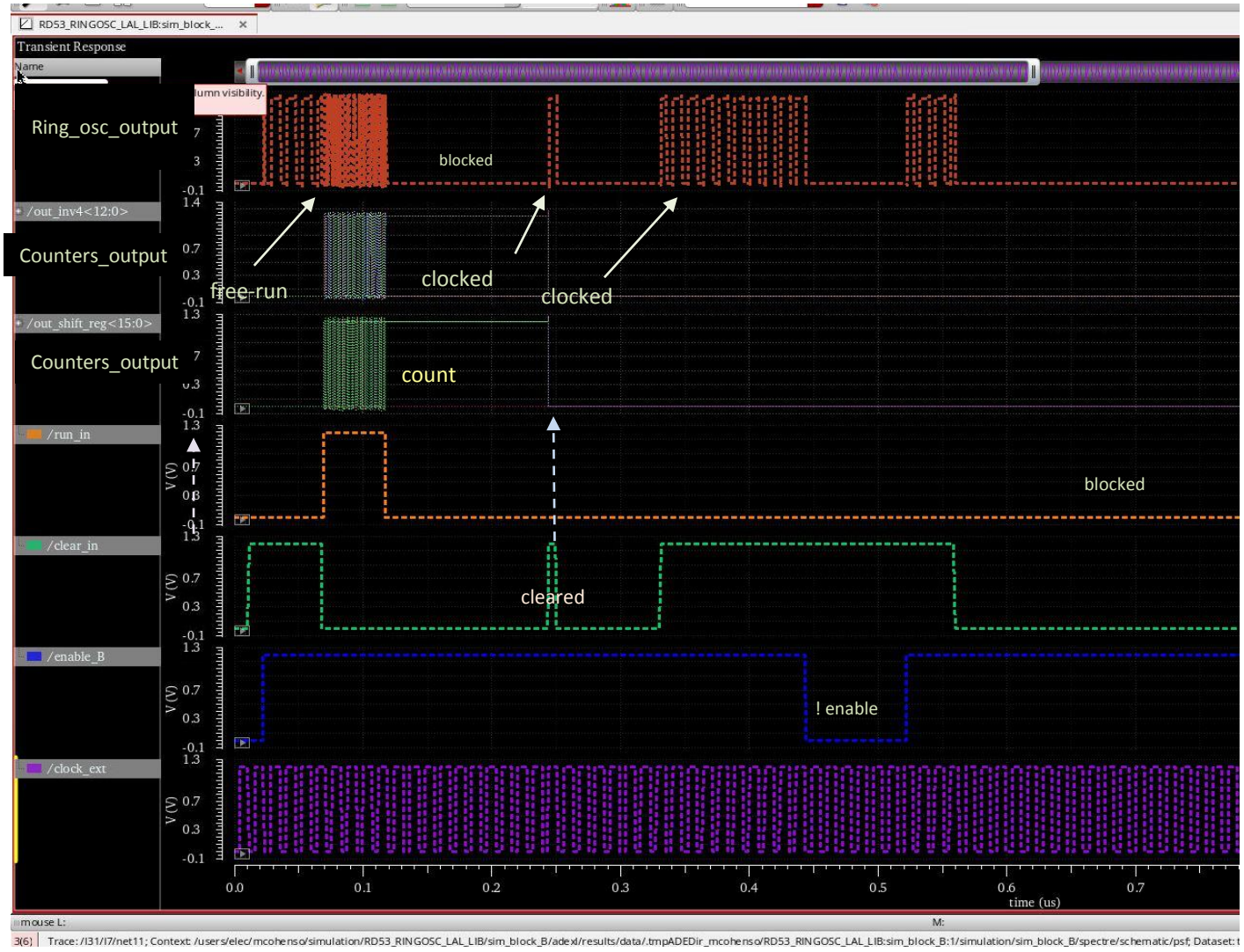
Counters_output



Counters_output

(Maurice c s, Kostiantyn Sakhatskyi)

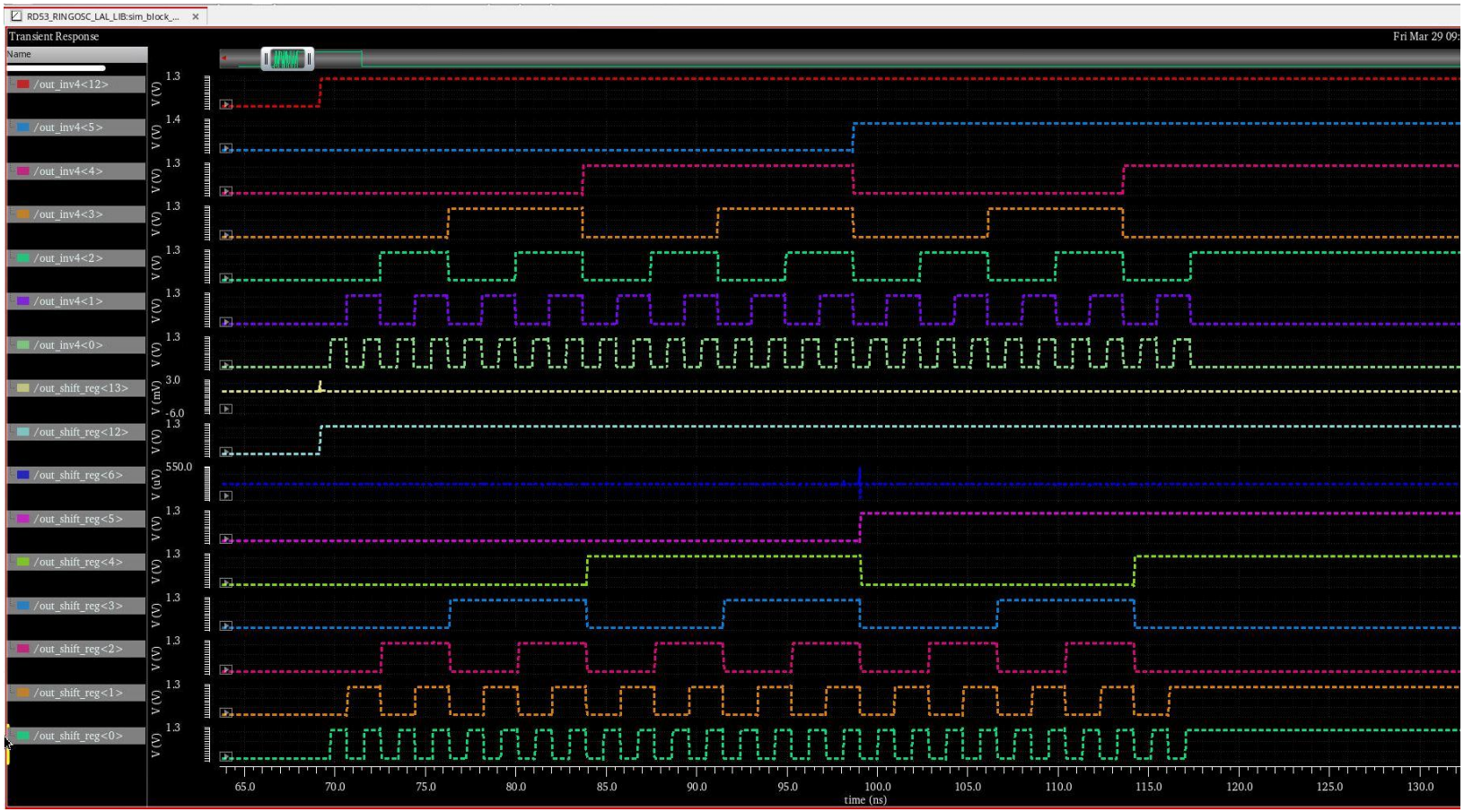
RD53B Simulation *[ring_oscs + counters]*



(Maurice c s, Kostiantyn Sakhatskyi)

RD53B Simulation *[block_B simulation ; counters zoom]*

Counters_output



Counters_output

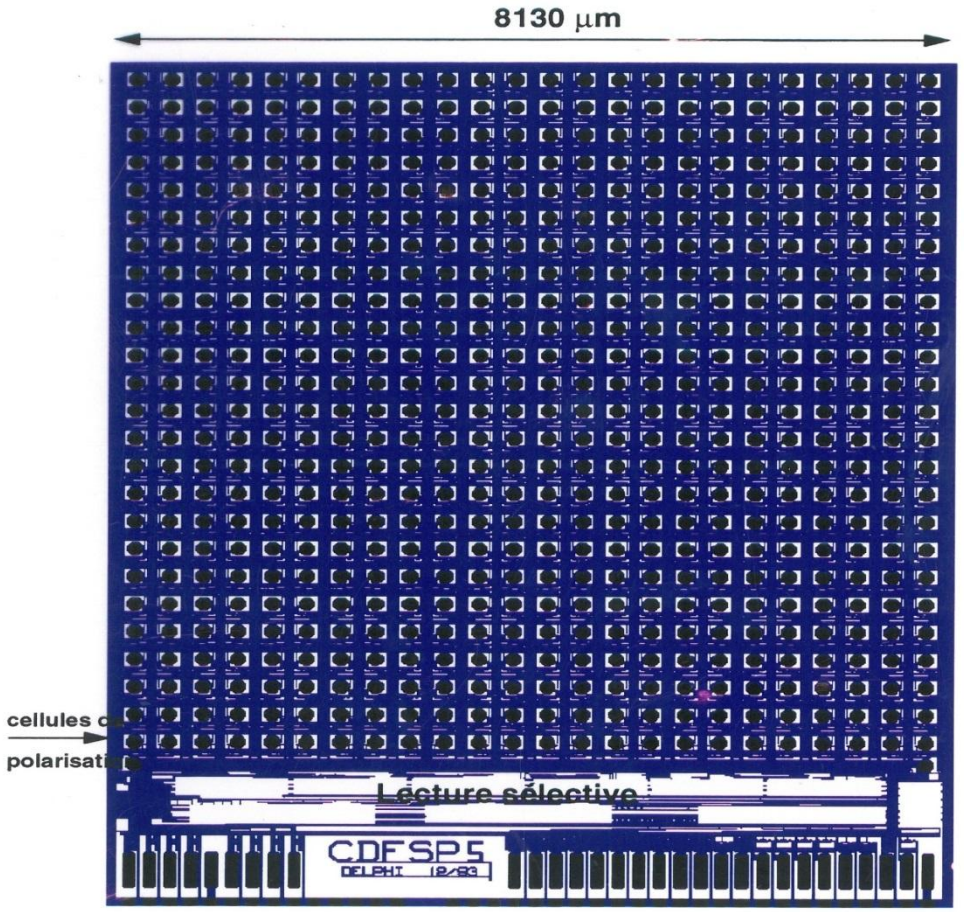
(Maurice c s, Kostiantyn Sakhatskyi)

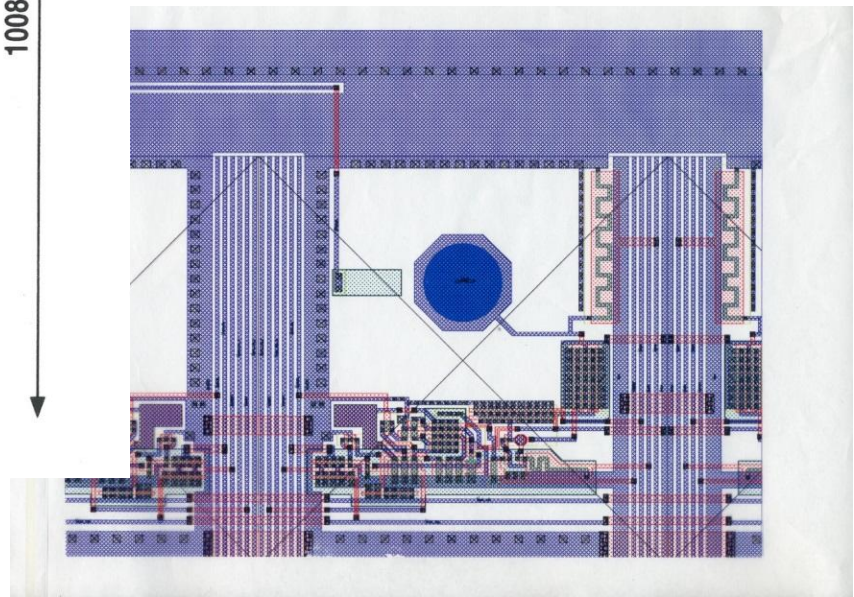
DELPHI

Architecture de la puce

24 x 24 voies d'électroniques

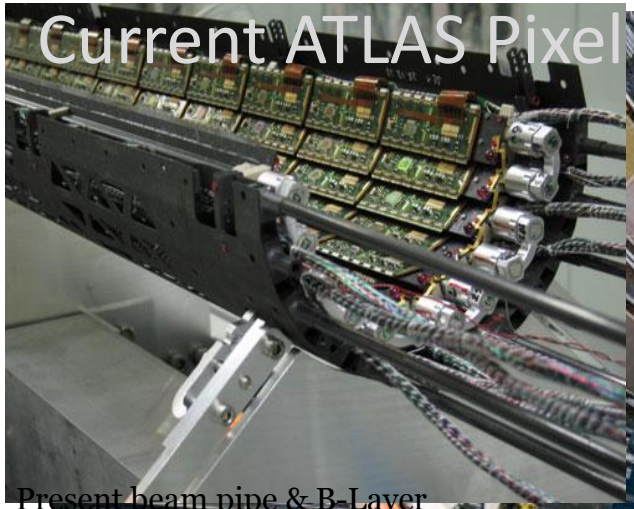
90 μm rms

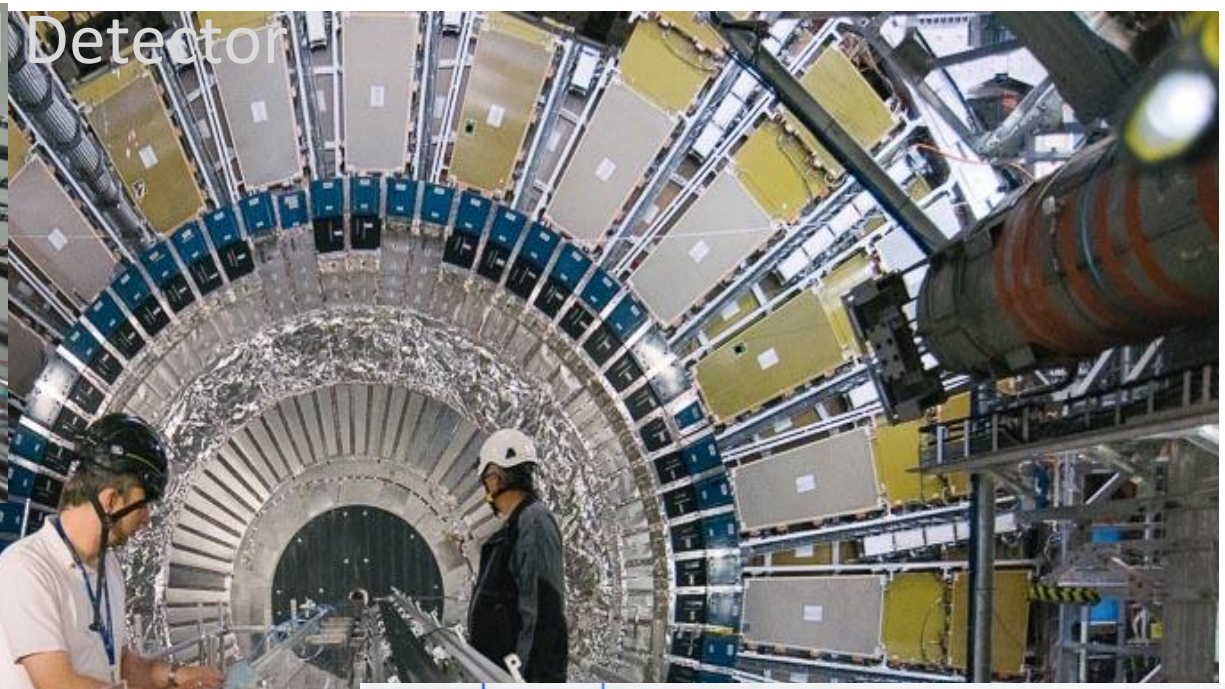




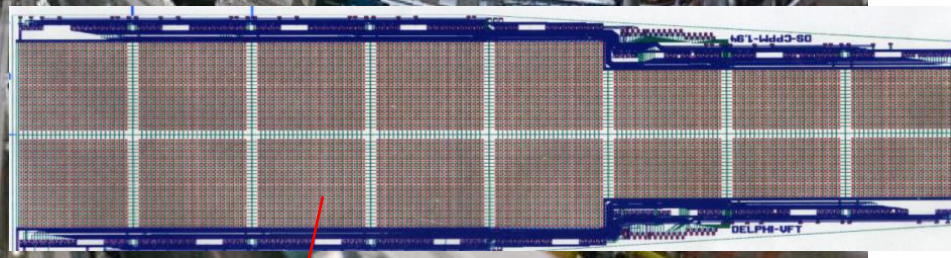
solal@lal.in2p3.fr

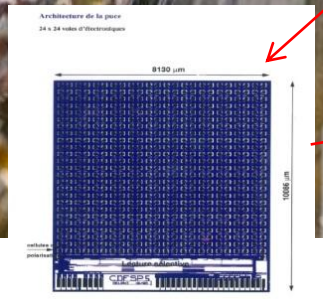
Current ATLAS Pixel Detector

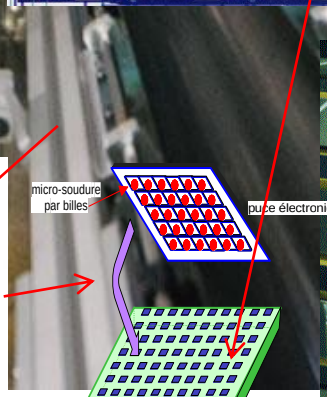


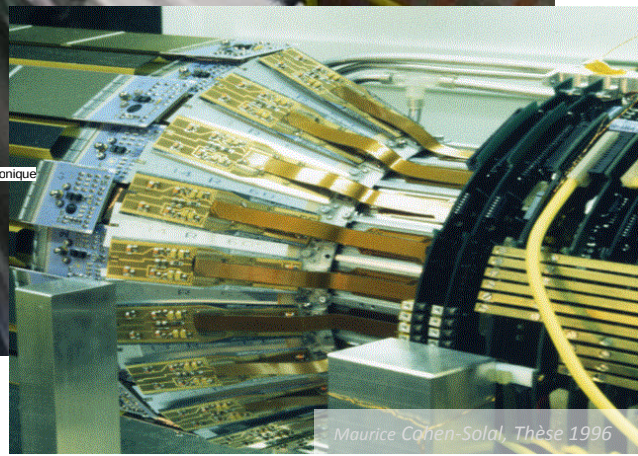


Present beam pipe & B-Layer



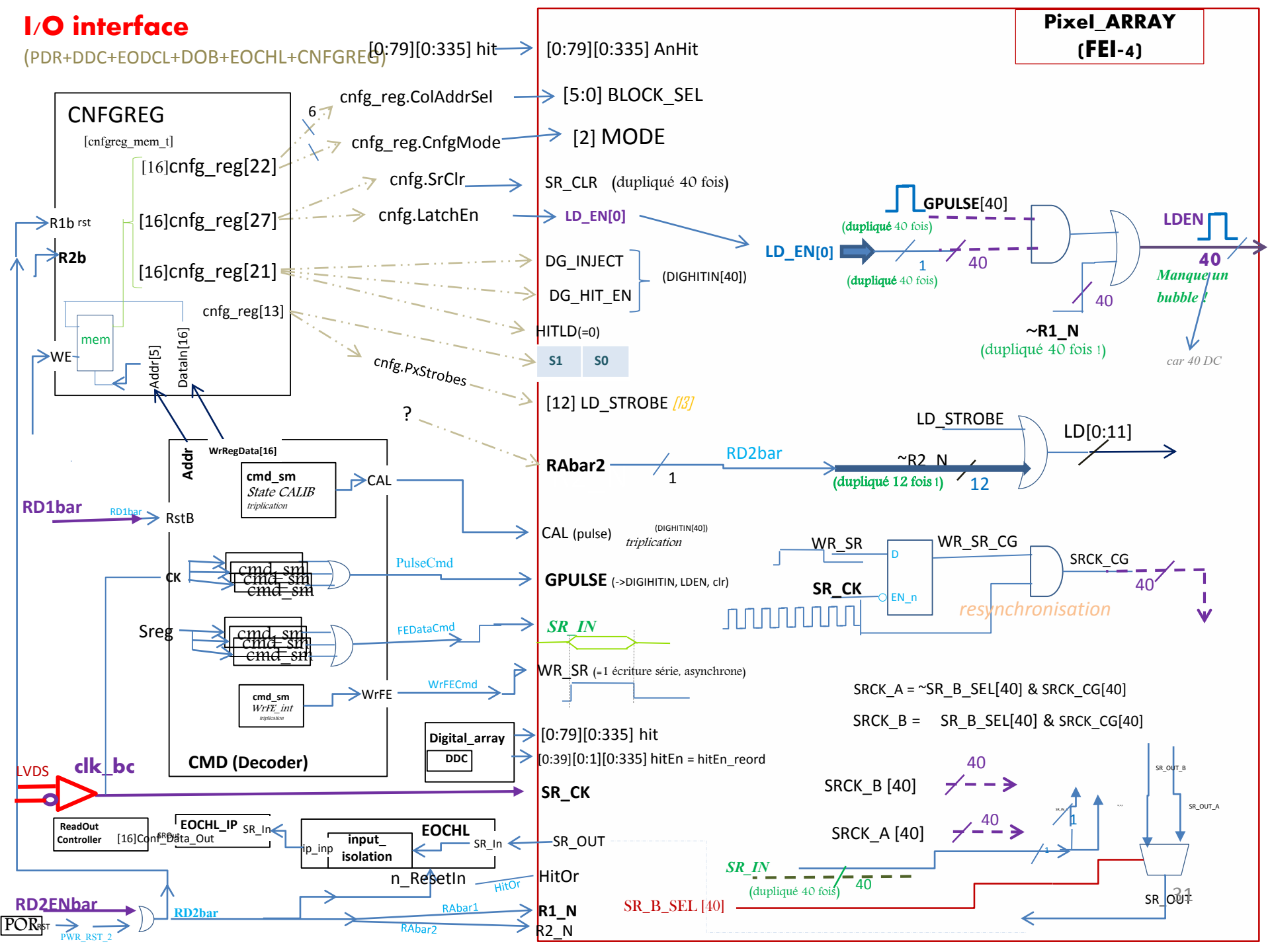






Maurice Cohen-Solal, Thèse 1996


Détecteur de Traces interne ATLAS
** Technologie Pixels **


I/O interface
(PDR+DDC+EODCL+DOB+EOCHL+CNFGREG)
Pixel_ARRAY
(FEI-4)
[0:79][0:335] hit
[0:79][0:335] AnHit
CNFGREG
[cnfgreg_mem_t]
cnfg_reg.ColAddrSel
[5:0] BLOCK_SEL
6
cnfg_reg.CnfgMode
[2] MODE
[16]cnfg_reg[22]
cnfg.SrClr
SR_CLR (dupliqué 40 fois)
[16]cnfg_reg[27]
cnfg.LatchEn
LD_EN[0]
R1b rst
R2b
[16]cnfg_reg[21]
DG_INJECT
DG_HIT_EN
(DIGHITIN[40])
cnfg_reg[13]
mem
WE
Addr[5]
DataIn[16]
HITLD(=0)
S1
S0
cnfg.PxStrobes
[12] LD_STROBE [13]
?
Addr
WrRegData[16]
RAbar2
RD1bar
RstB
cmd_sm
State CALIB
triplication
CAL
CAL (pulse)
(DIGHITIN[40])
triplication
CK
PulseCmd
GPULSE (->DIGIHITIN, LDEN, clr)
Sreg
FEDataCmd
SR_IN
WrFECmd
WR_SR (=1 écriture série, asynchrone)
cmd_sm
WrFE_int
triplication
WrFE
Digital_array
DDC
[0:79][0:335] hit
[0:39][0:1][0:335] hitEn = hitEn_reord
CMD (Decoder)
LVDS
clk_bc
SR_CK
ReadOut
Controller
[16]Conf_Data_Out
EOCHL_IP
SR_In
ip_inp
input_
isolation
EOCHL
SR_In
SR_OUT
n_ResetIn
HitOr
RD2ENbar
POR
PWR_RST_2
RD2bar
RAbar1
RAbar2
R1_N
R2_N
GPULSE[40]
(dupliqué 40 fois)
LD_EN[0]
1
40
(dupliqué 40 fois)
LDEN
40
Manque un
bubble !
40
~R1_N
(dupliqué 40 fois !)
car 40 DC
LD_STROBE
LD[0:11]
RD2bar
~R2_N
1
(dupliqué 12 fois !)
12
WR_SR
D
WR_SR_CG
SRCK_CG
40
SR_CK
EN_n
resynchronisation
SRCK_A = ~SR_B_SEL[40] & SRCK_CG[40]
SRCK_B = SR_B_SEL[40] & SRCK_CG[40]
40
SRCK_B [40]
40
SRCK_A [40]
SR_IN
(dupliqué 40 fois)
40
SR_B_SEL [40]
SR_OUT_B
SR_OUT_A
SR_OUT
21

One pixel configuration

FEND_PIX_DIGI

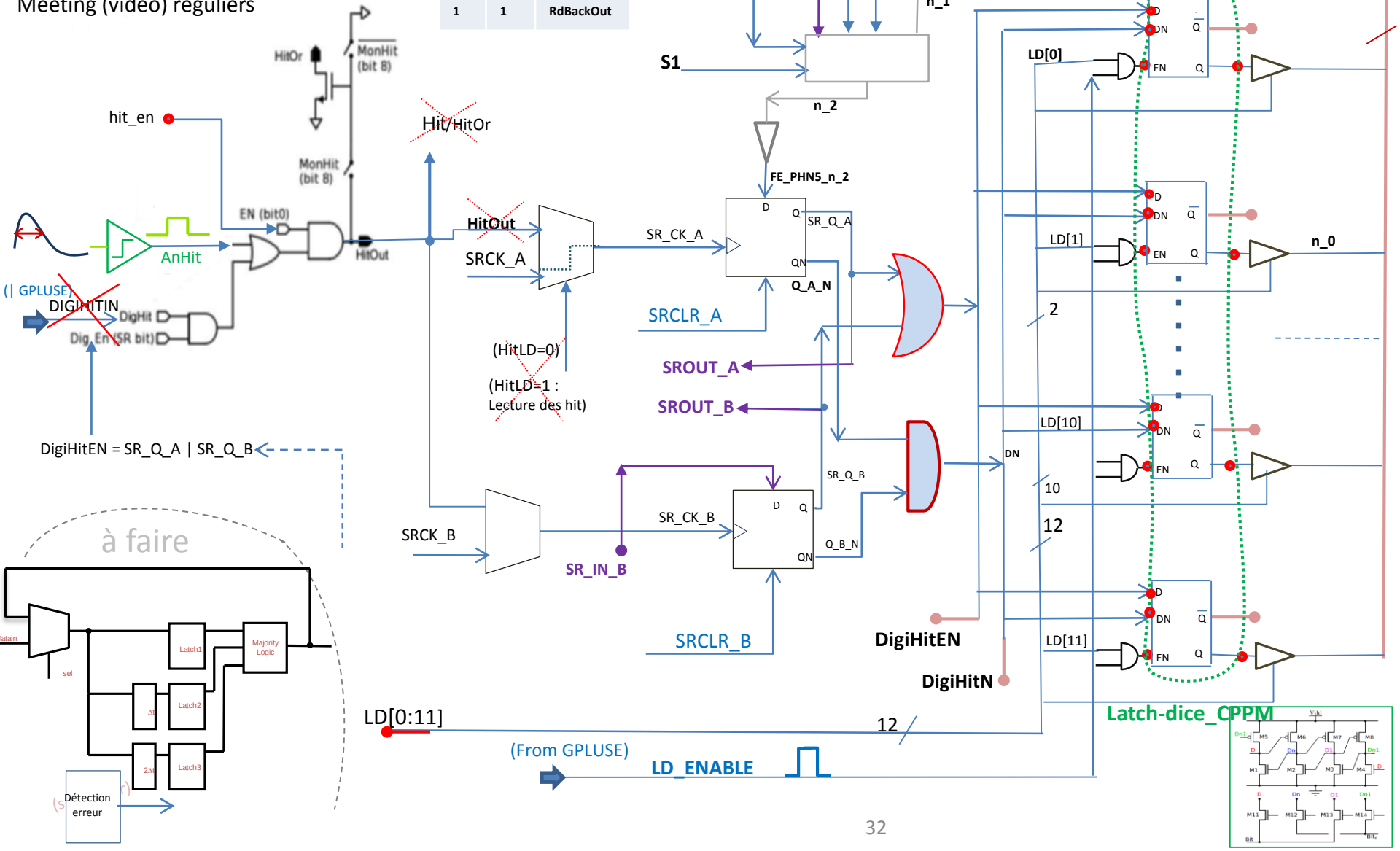
Collaboration avec CPPM Marseille (dec.14- **oct.15**)

Moshine Menouni & Denis Fougeron

Meeting (vidéo) réguliers

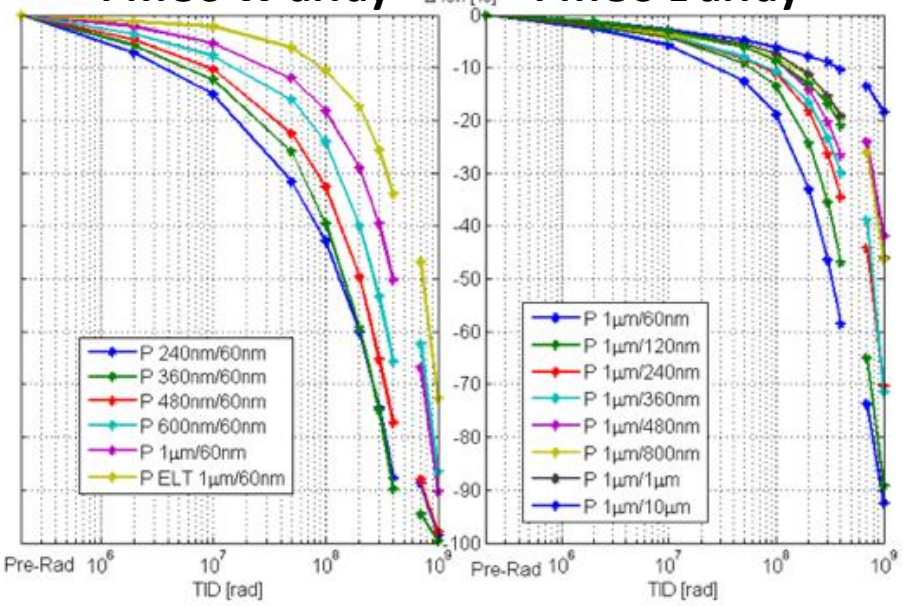
(HitLD=0)

S1	S0	SR_D_A
0	0	SRIN_A
0	1	1
1	0	0
1	1	RdBackOut

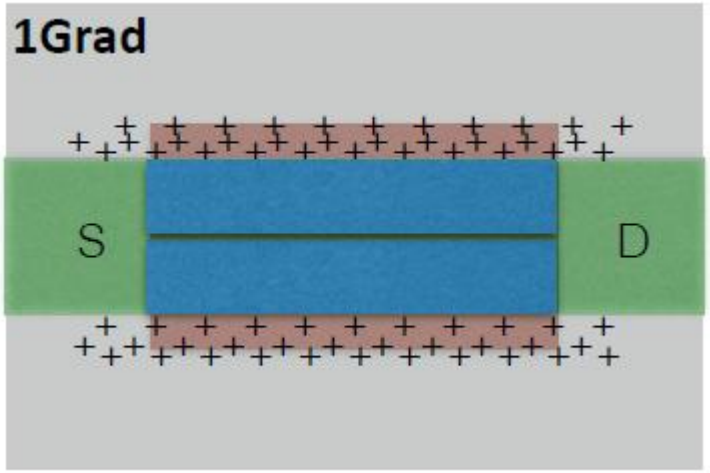


WG1 : Radiation

PMOS W array **PMOS L array**

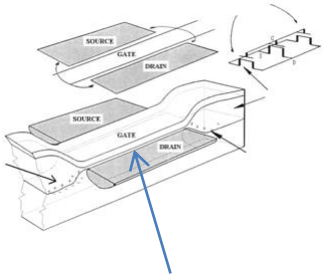


Enrichir avec Status65nm_ap…



Recommandations analog block :

–**PMOS W≥300nm, L≥120nm** ; NMOS L≥120nm → **puissance, surface, performa**
–Travail présent : **Modélisation** (extraction de paramètres "Radiation corner").



Lateral **D**iffusion

SEU

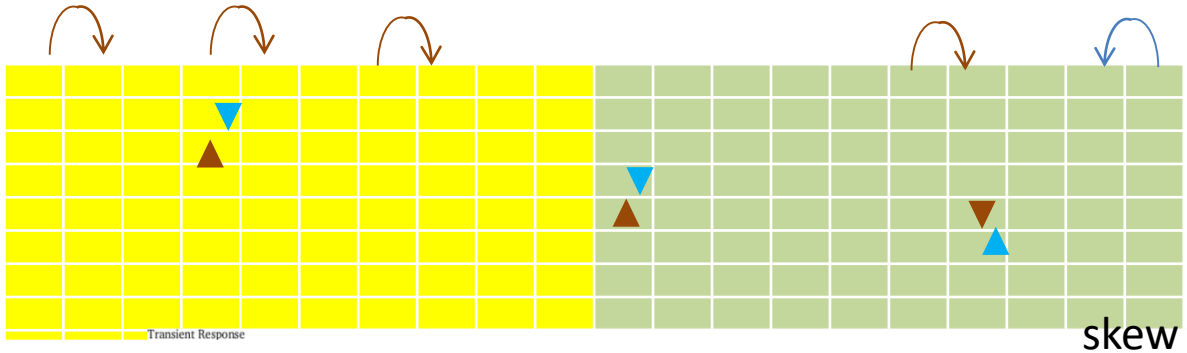
TRL with delays

		Error rate Number of errors/ spill		
	area	0 to 1	1 to 0	All
DFF for shift register	14.4 µm²	5.6	2.9	4.2
TRL for configuration	40 µm²	0.082	0.04	0.06
TRL + delay	54 µm²	0.064	0.015	0.04

Optimisation buffers & lines for 1 column of 400 pixels

LAYOUT ≡ 20 LIGNES X 20 COLONNES = 400 PIXELS

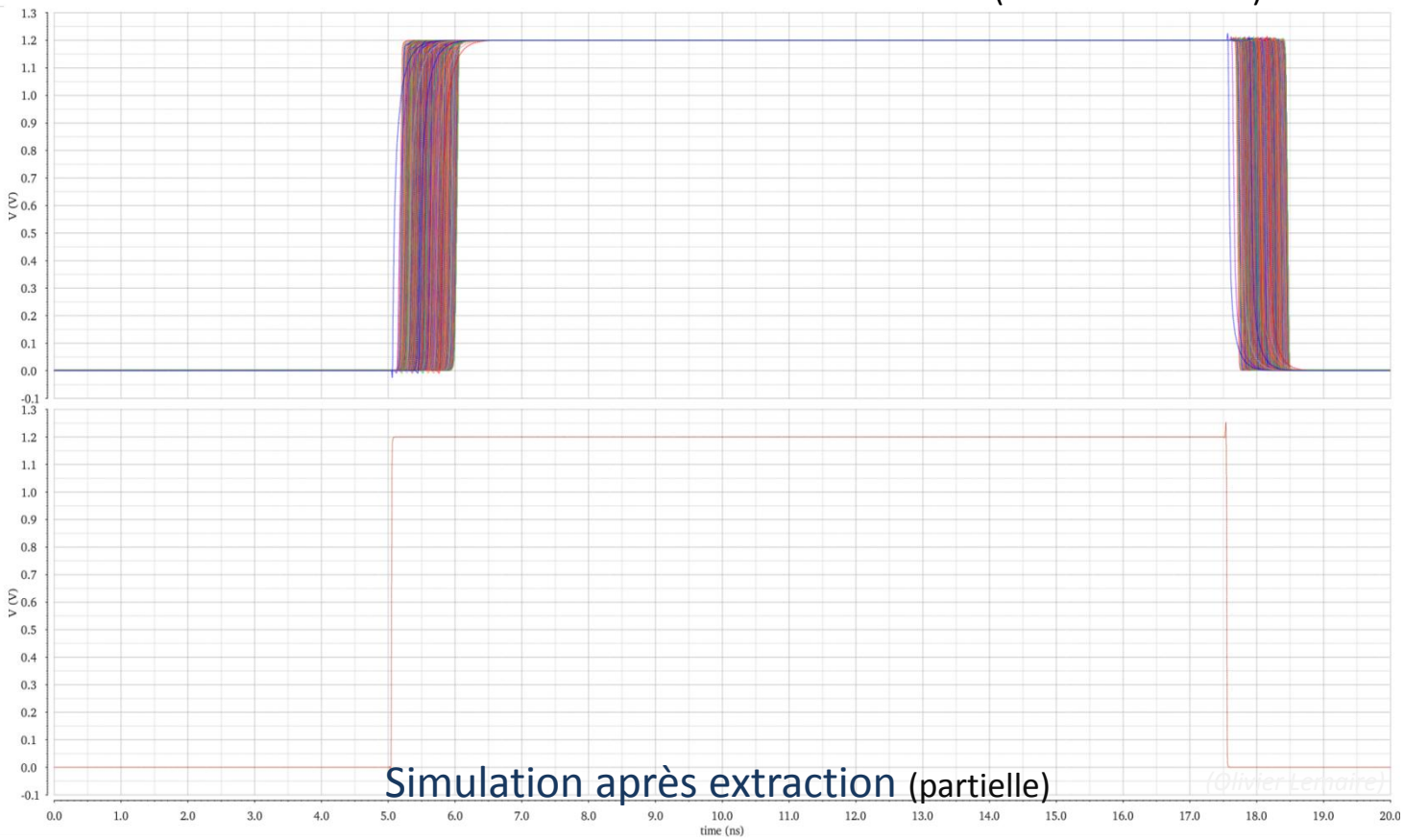
1 mm x 1 mm pitch **50µm x 50µm**



Clock : length line 400 x 50 µm = 20 mm !

Correction cellule dans le code synthétisé

skew = 2 nsec (**extraction totale**)



Simulation après extraction (partielle)

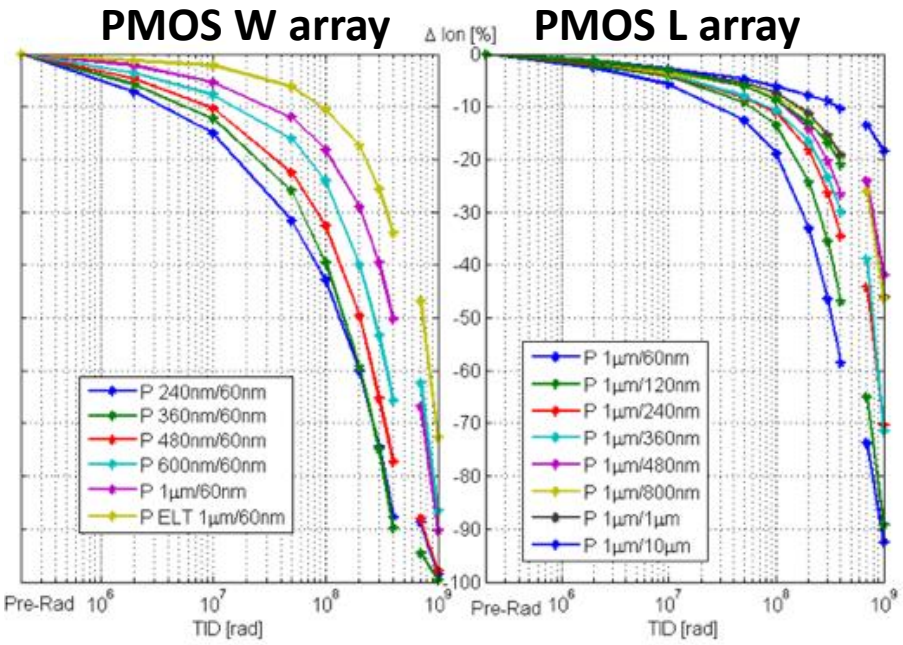
Optimized under Virtuoso

Do not use higher metals
(too width)

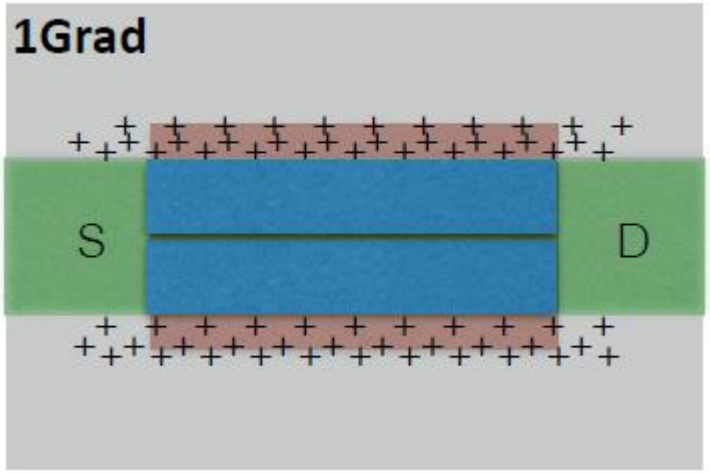
Optimum found :
buffer each 40 pixels

(The buffers are inside the pixel)

WG1 : Radiation



Enrichir avec Status65nm_ap…



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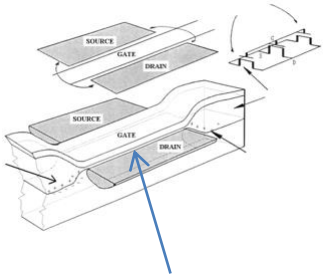

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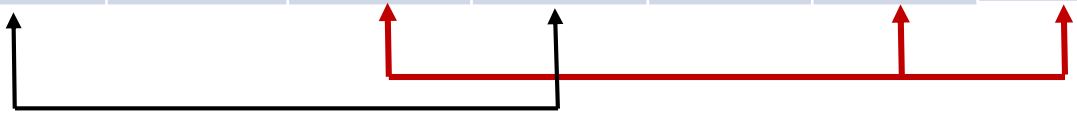
Extracted simulations & measurements frequencies

Version A

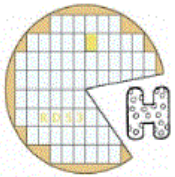
f_{osc} [MHz]

	Simulations schematic		Simulations extracted			Measurements at CERN			Measurements at LAL	
Flavours	T = +27°C VDD = 1.2V	T = - 20°C VDD = 1.2V	T = +27°C VDD = 1.2V	T = - 20°C VDD = 1.2V	T = - 10°C VDD = 1.13V	Room T° VDD = 1.2V	Room T° VDD = 1.12V	T = -10°C VDD = 1.13V	T = - 10°C VDD = 1.12V	T = - 20°C VDD = 1.12V
CKND0	887	933	502	524	462	408	352	395	398	406
INVD0	895	940	478	499	438	392	337	377	383	390
NAND4D0	869	918	483	506	435	383	322	372.5	372	380
NOR4D0	912	960	545	569	487	420	349	406	406	416
CKND4	889	936	660	691	608	645	556	630	630	642
INVD4	897	946	648	679	598	631	543	613	616	627
NAND4D4	914	969	686	726	624	658	554	623	641	655
NOR4D4	906	940	687	717	615	645	538	614.5	625	639



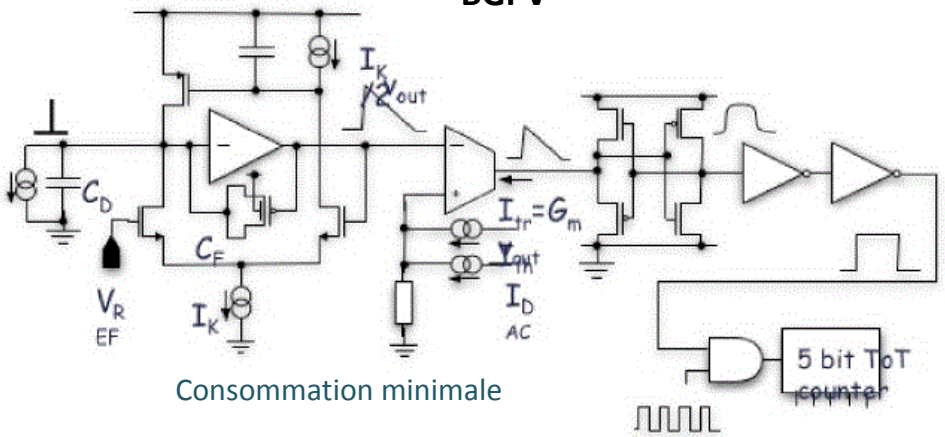
(Maurice, Moshine, Olivier, Luis, Vasyl, Jimmy, Abdénour)

Une amusoire →



INFN-Pavia design (& Bergamo)

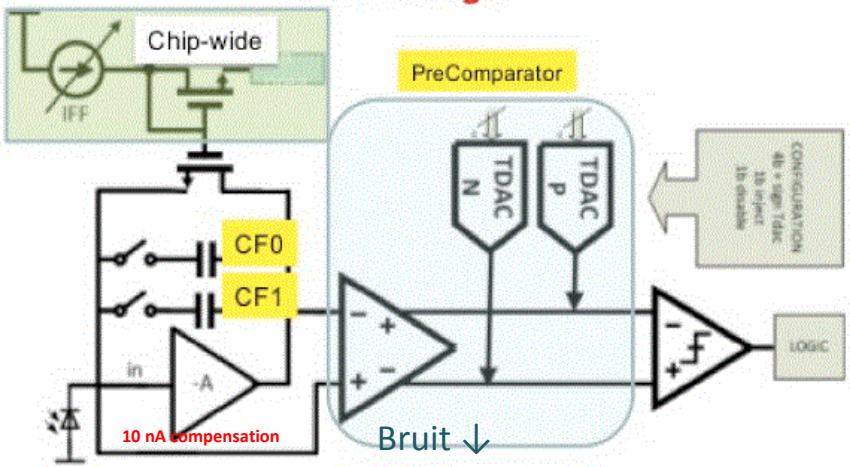
BGPV



Consommation minimale

Single stage with current comparator and ToT counter

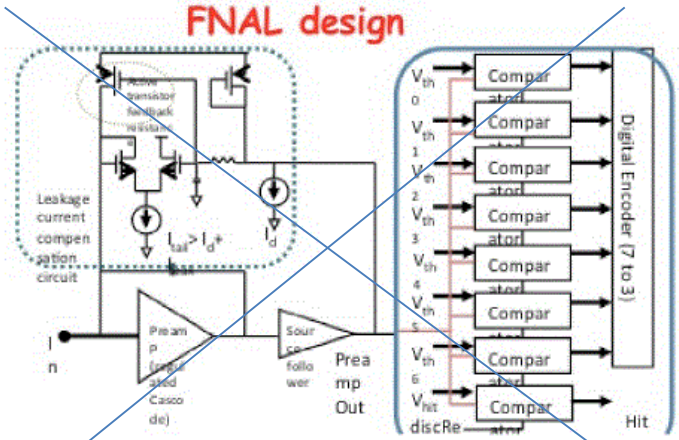
LBNL design



Bruit ↓

1 of 4 in quad "analog island" of FE65_P2

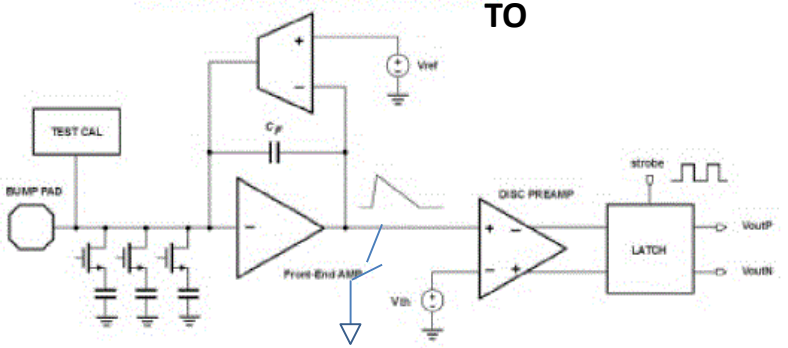
FNAL design



Synchronous: resets every bunch crossin. Flash ADC

INFN-Torino design

TO



Single stage with SAR-like ToT counter using synchronous comparator

fast

RD53A chip

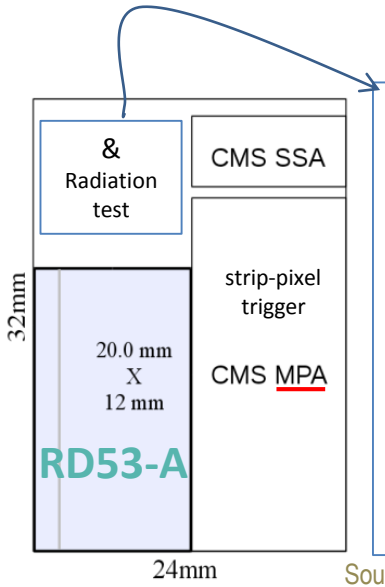
- ## MPW – Multi-Project Wafer

price ~ 90% engineering run (Full Maskset)

Mini ASIC 2mm x 2mm = 17 000€ + 1 000€

(C3) → 1 mm x 1mm = ¼ (18 000) = 5 150 €

(RD53-A) → 20 mm x 12mm **~ 500 k€**



- **FE65-P2 and Chipix65B:** RD53A front end prototypes, modified
- **Pixcap65:** to precisely measure sensor capacitance components
- **Pixfel:** a prototype hybrid pixel readout chip for free electron laser detectors
- **Clicpix:** 25u x 25u pixel readout chip prototype

Soumis fin de semaine dernière
Retour novembre 2017

- ## MLM – Multi Layer Mask

- NRE (Non-Recurring Engineering) ↘ wafer price ↗

220 k$ / mm²

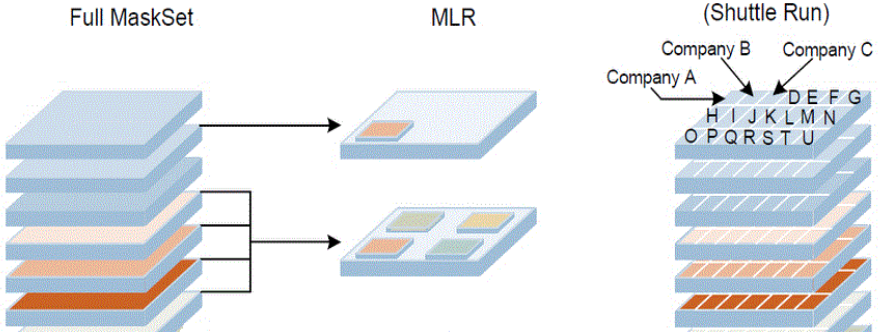
2 wafers 6 ''
~ 40 chips

- ## Engineering Run

Wafer nécessaire pour le bump bonding

(RD53-A) → 20x12 mm² ≡ ~ 1 M€

(RD53) → 400 mm² ≡ 2,2 M€

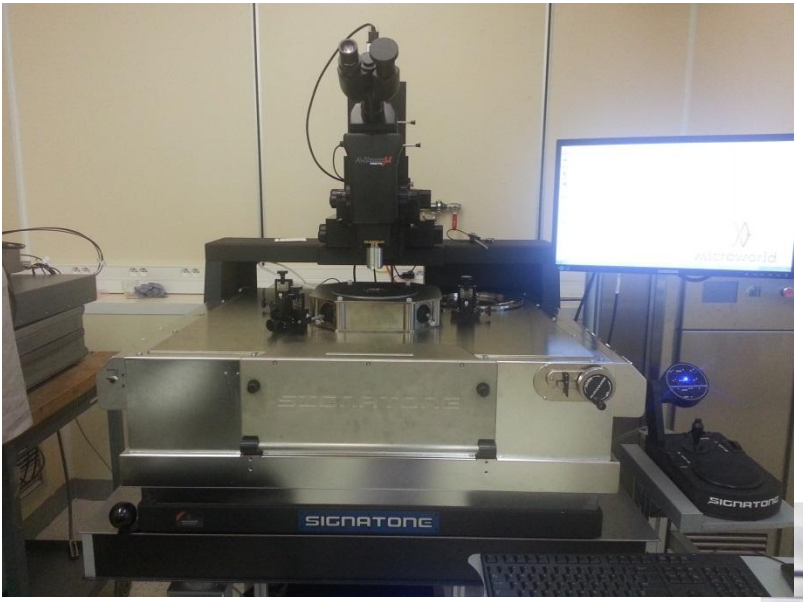


(~ 6 wafers min)

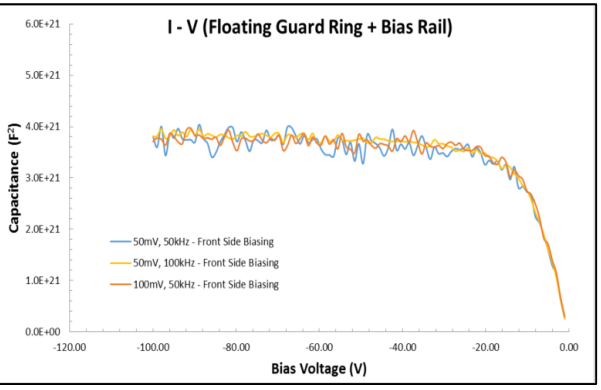
Sigmatone

SEMI AUTOMATIC PROBE STATION

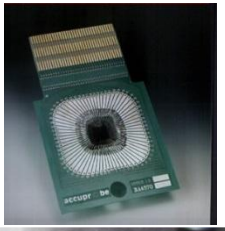
New 50 m2 cleanroom with acquisition of semi-automatic testing system machine.
For medium or large scale testing, such as for the HL-LHC.

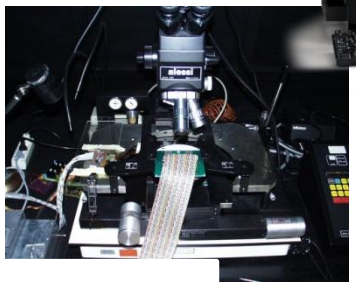


Measurement
from -60 °C to 300 °C



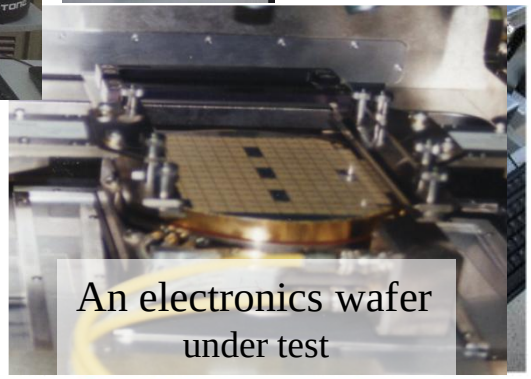
Test, caractérisation & appariement



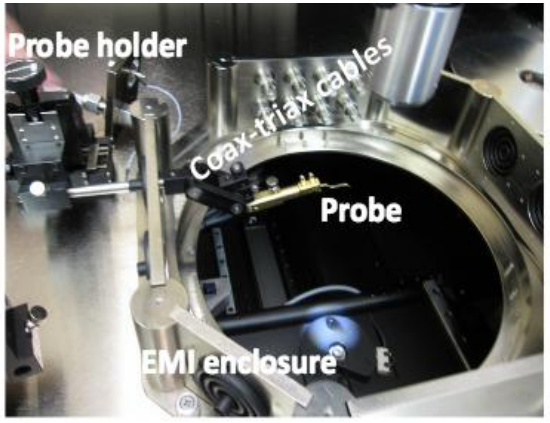


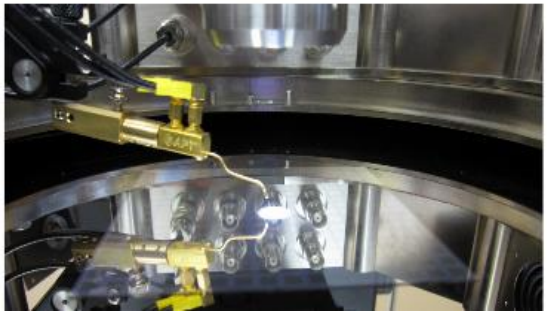
KEITHLEY
A Tektronix Company

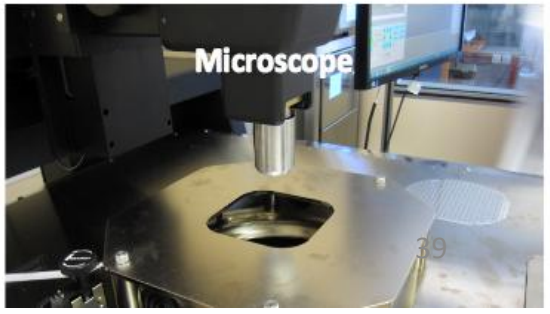
Test de semi conducteur



An electronics wafer
under test







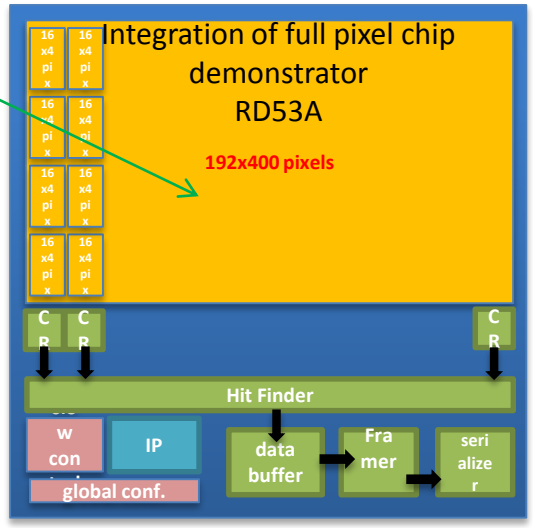
Top Level Integration

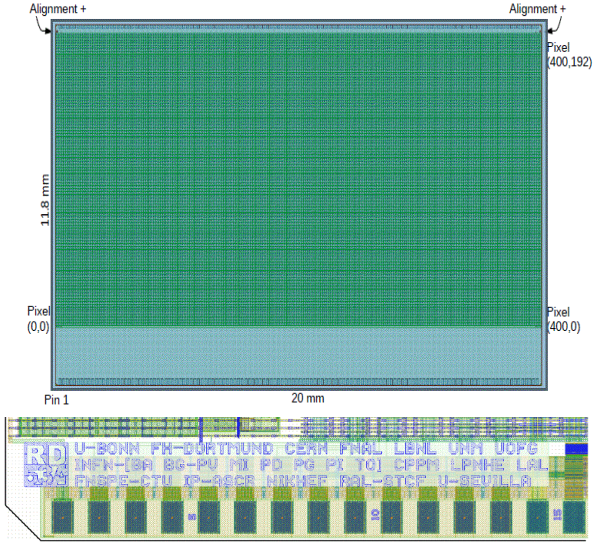
RD53-A ATLAS-Itk-Pixel

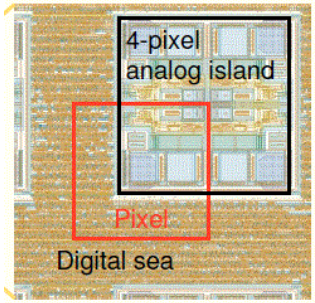
Analogue Front End

128 col. TO (16x8)	136 col. BG-PV (17x8)	136 col. LBNL (17x8)

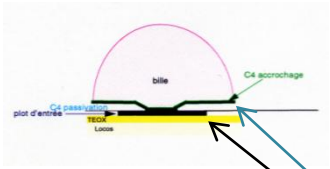
Métaux :
7 thin, 1 thick, 1 UTM, RDL + RDL



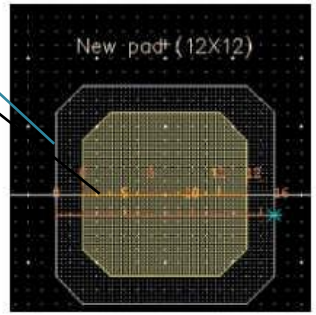




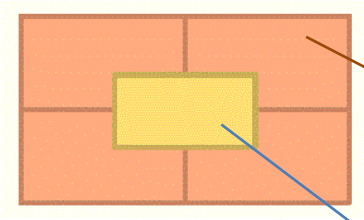
Pixel region with digital sea and analog islands



Bump bonding



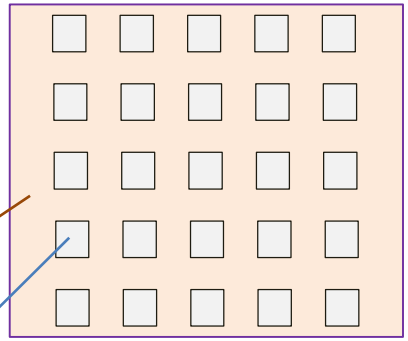
Ouverture



50 x 250 µm²
130 nm
Type FEI-4

Digital

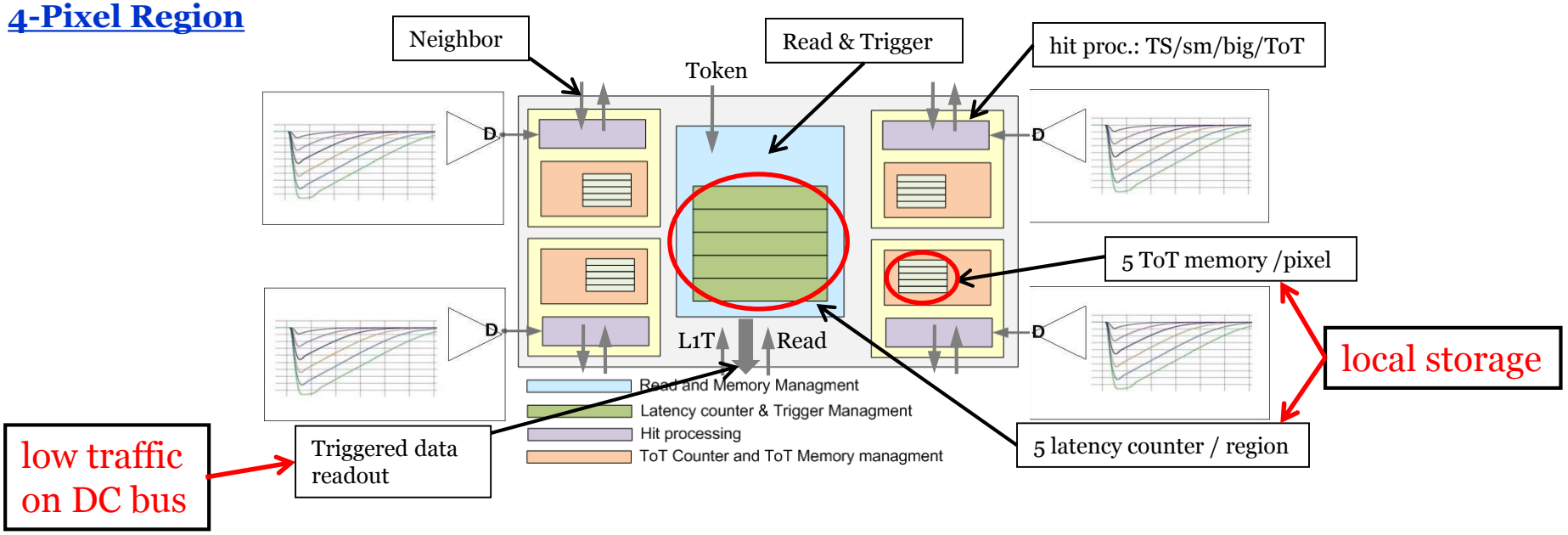
analog



50 x 50 µm²
65 nm
Type RD53

Digital Pixel: Regional Architecture

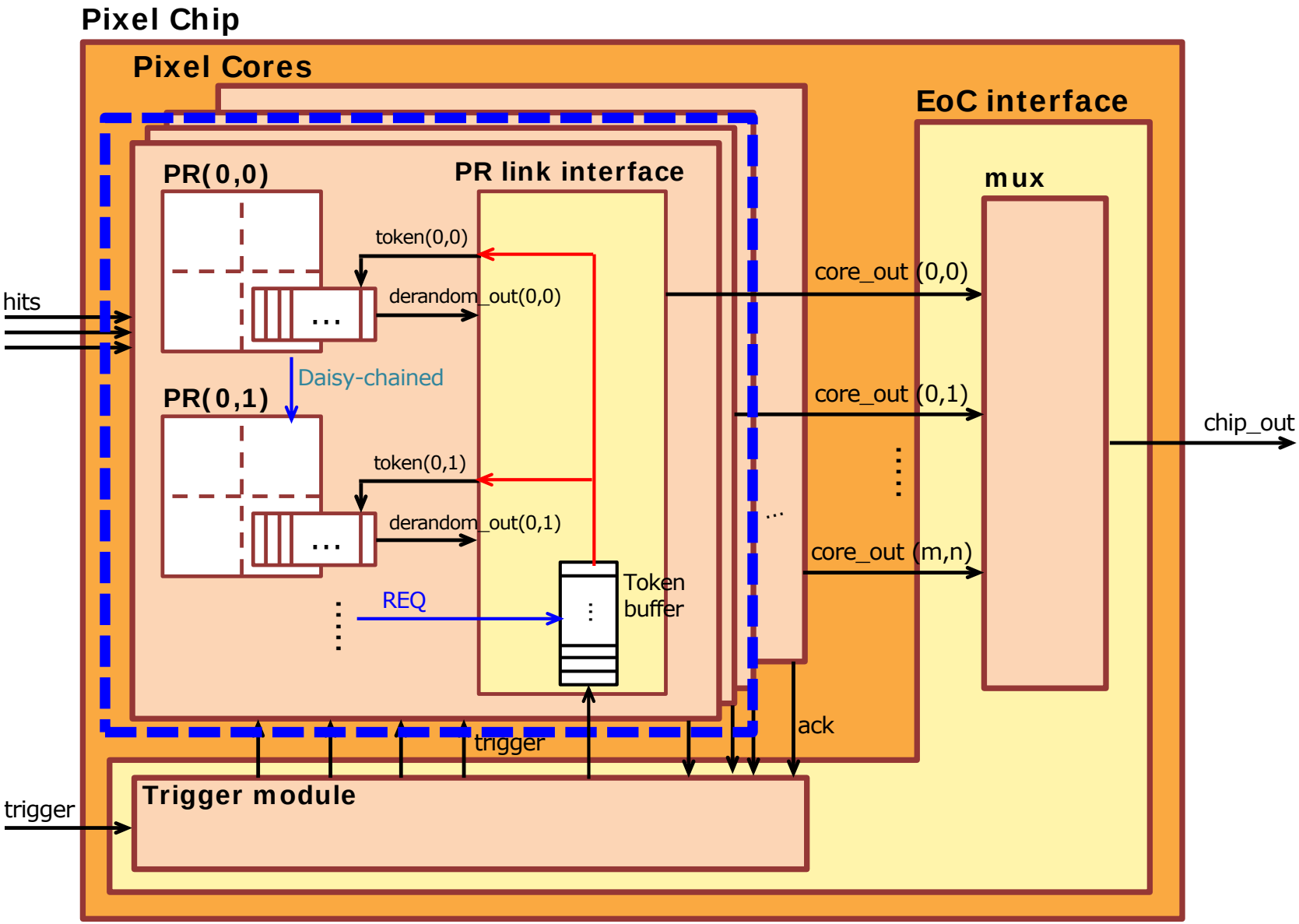
4-Pixel Region



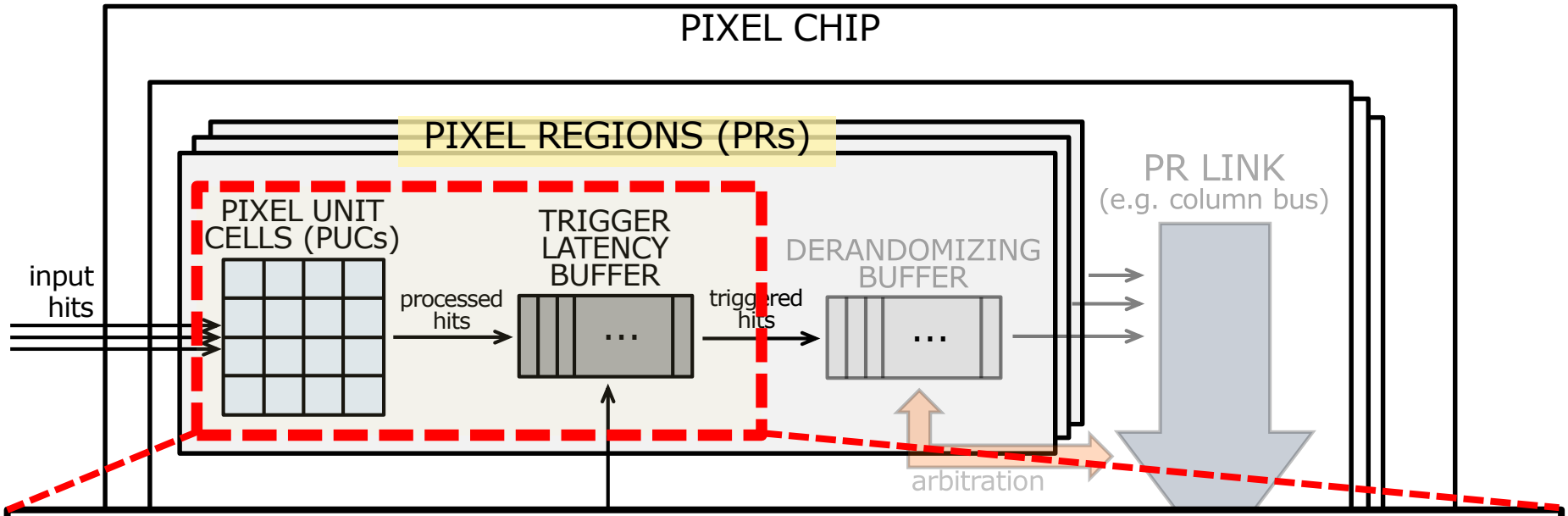
- Store hits locally in region until L1T.
- Only 0.25% of pixel hits are shipped to EoC → DC bus traffic "low".
- Each pixel is tied to its neighbors -time info- (clustered nature of real hits). Small hits are close to large hits! To record small hits, use position instead of time. Handle on TW.

Summary:

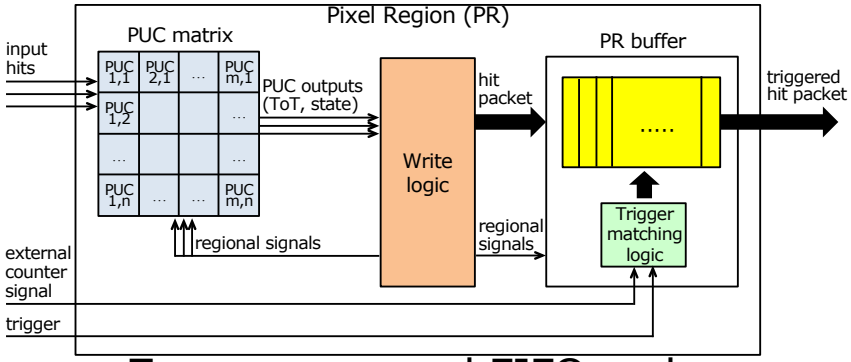
- Physics simulation→Efficient architecture.
- Spatial association of digital hit to recover lower analog performance.
- Shared resources & hit not moved around → Lowers digital power consumption.


Pixel Chip
Pixel Cores
EoC interface
PR(0,0)
PR link interface
mux
token(0,0)
hits
derandom_out(0,0)
core_out (0,0)
Daisy-chained
PR(0,1)
core_out (0,1)
chip_out
token(0,1)
derandom_out(0,1)
core_out (m,n)
Token
buffer
REQ
ack
trigger
Trigger module
trigger

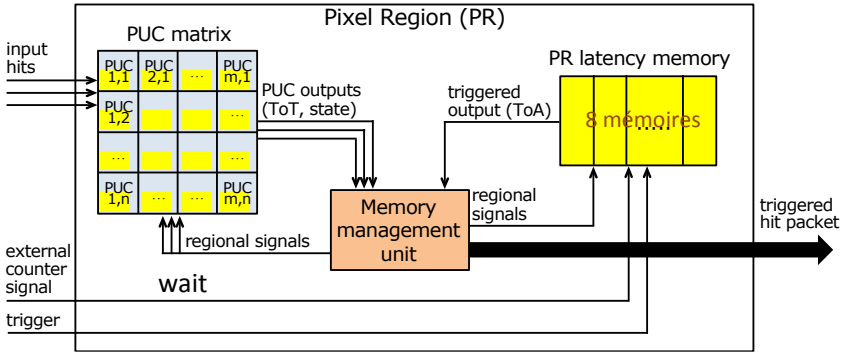
Current scheme *(i.e. "Wait Then Transfer")*



1. Focus on trigger latency buffering

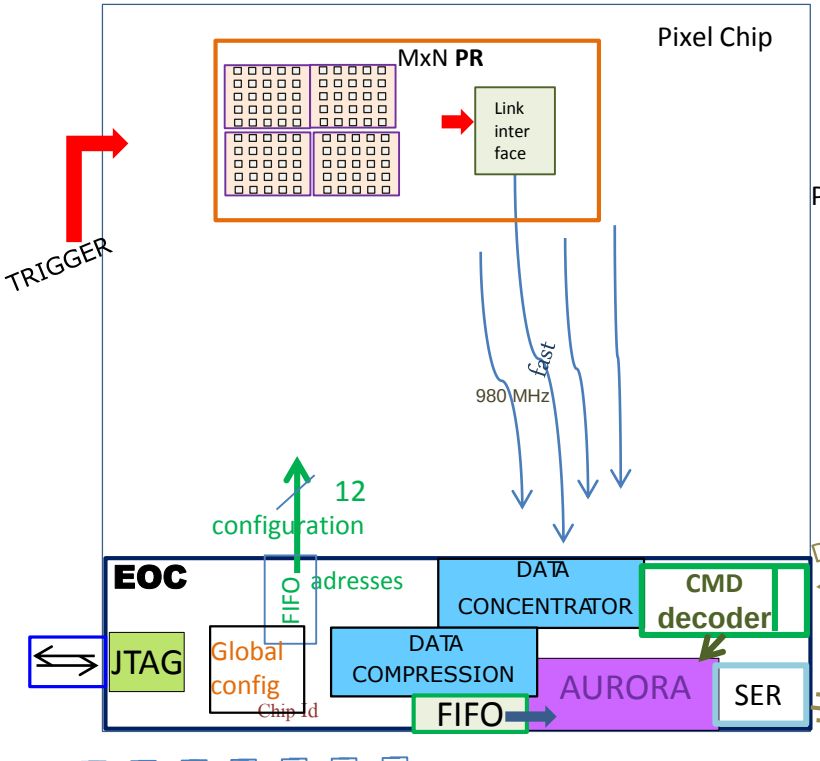


~~Zero-suppressed FIFO arch.~~



Distributed latency counters arch.

Pixel chip model & I/O



MN PRs = PRs = 1 Pixel Core

Pixel Chip = Pixel Cores + End of Core

1 stave = 13 modules

(modules : 4 chips)

From other detector physical regions (different timing)

1

(DC balanced sur 8 bit ou 16 bit)

Down link

serial

(control, incommingcommand)

SubLVDS

concentrator

FPGA

lpGiBiTr

LC osc.

Speed reducer

shielded

4metal

63 Pixel Data Frame

Optic fibre

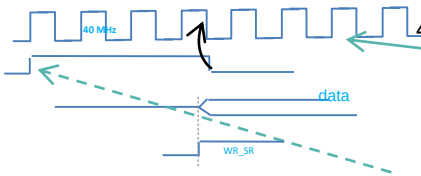
10 (or 20) Gb/s

~ 40 m

Aurora (640Mbps/trame)

(OUTPUT stream) Current Mode Logic

jitter ?



40 MHz

Clock D. recovery (jitter<30ps)

PLL (160, MHz) ; stabilité ?

Système lock (40MHz)

Phase lock (Programmable 1.5ns)

Désérialiseur

Command decoder

Décodeur Hamming

Adress decoder

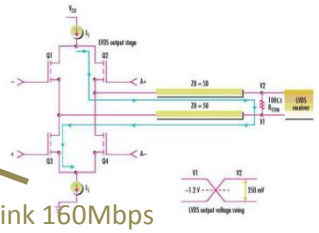
Calibration (latence, …)

Configuration & commandes

20 Mbps

Trigger

arbitraire



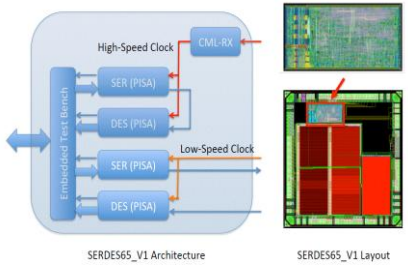
Down link 160Mbps

Encoded Hamming 4 ou 8 bits

(the bandwith must increased)

Down link (stave)

4.2 Gb/s



Experiment

Cahier des charges ATLAS-Itk-Pixel I/O

Scan chain control

PU

EOC EOC EOC

P Core

fast

Merge

EOC

DOB FIFO

SER 1:20

J-tag

Down link

160 Mb/s

control

Sortie Aurora

Up link

5.12 Gb/s

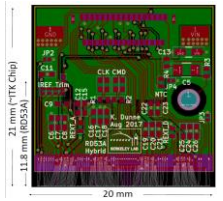
2.4 Gb/s

(programmable ; ÷ 1, 2, 4, 8, 16)

Erreur $<10^{-12}$

2-bit

Carte FE pour quad



1 stave = 13 modules

(modules : 6x 4 chips)

(quad)

FPGA

ASIC

or in the FE

concentrator

LPGBT

Optical converter

Optic fibre

Speed reducer

Radiations 1GRad

10 (or 20) Gb/s

~ 40 m

Down link (stave)

4.2 Gb/s

Experiment

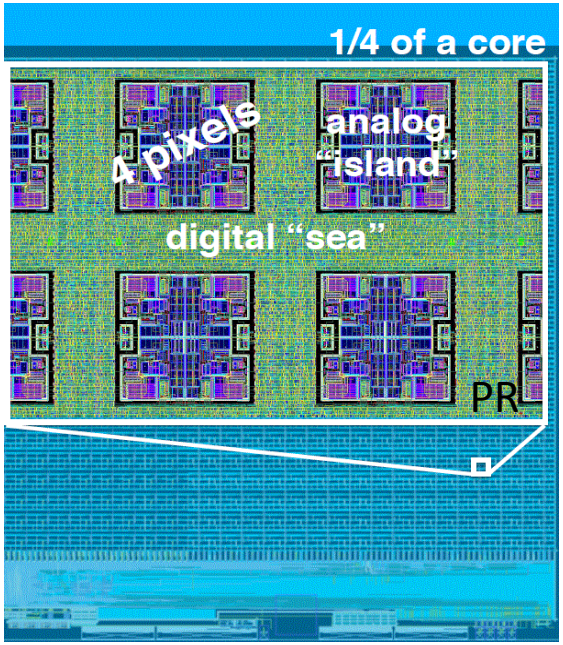
Pixel Region (PR)

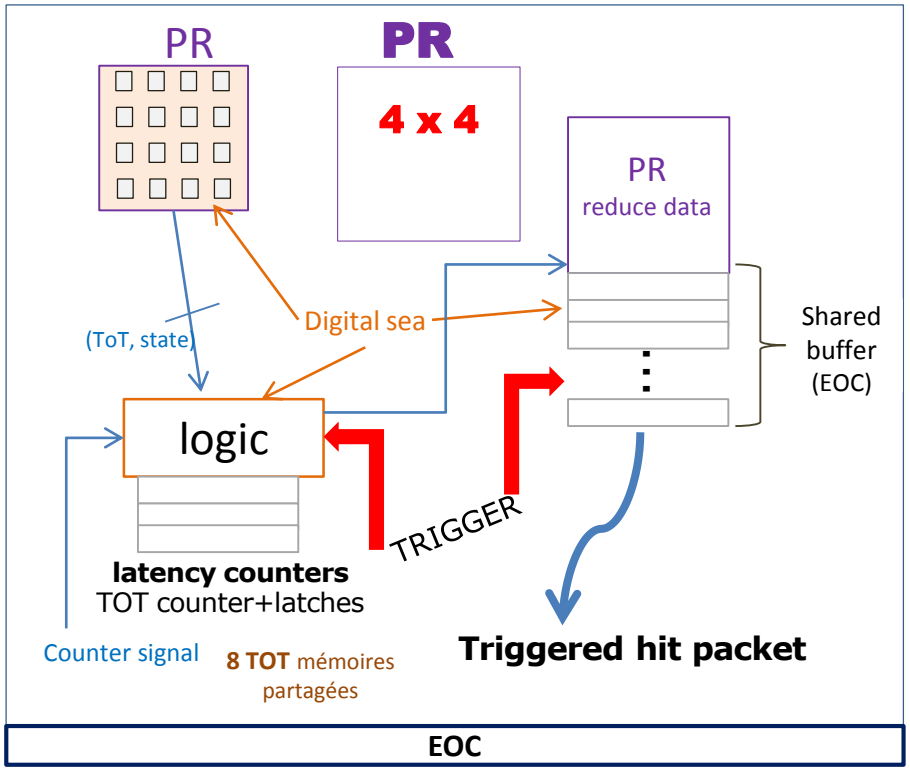
RD53A : **196 rows x 400 columns**
Soit 78 400 pixels

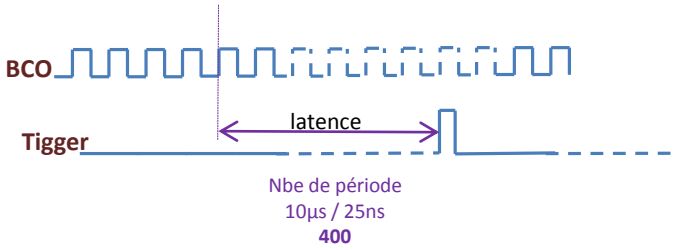
2 architectures possibles :

- Compteurs de latence distribués *(behavioural)*
- Zero supress FIFO *Hit loss*

Core = **4 x PR** = 8x8 pixels (inclut tout)







~ 40 bits par pixel dans la **PR**

Symbol Name	Encoding	Trigger Pattern	Symbol Name	Encoding	Trigger Pattern
			Trigger_08	0011_1010	T000
Trigger_01	0010_1011	000T	Trigger_09	0011_1100	T00T
Trigger_02	0010_1101	00T0	Trigger_10	0100_1011	T0T0
Trigger_03	0010_1110	00TT	Trigger_11	0100_1101	T0TT
Trigger_04	0011_0011	0T00	Trigger_12	0100_1110	TT00
Trigger_05	0011_0101	0T0T	Trigger_13	0101_0011	TT0T
Trigger_06	0011_0110	0TT0	Trigger_14	0101_0101	TTT0
Trigger_07	0011_1001	0TTT	Trigger_15	0101_0110	TTTT

15 **patterns** de commandes **trigger** (sur 4 Bunch Crossing ; indique quel(s) BCO est « triggered »)

(Autres)

Reset Compteur d'Evénements

Reset Compteur de BC

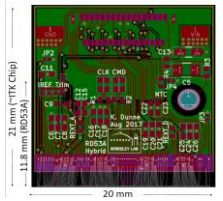
configuration

data[16]

AddCol [9]

Command	Encoding	ID/(A)ddress/(D)ata 5-bit Fields					
ECR	0101_1010	(contrôle de 8 CHIPS par câblage, broadcast)					
BCR	0101_1001						
Glob. Pulse	0101_1100	ID<3:0>,0	D<4:0>				
Cal DIG	0110_0011	ID<3:0>,0	D<4:0>	D<4:0>			
Cal ANA	0110_0011	ID<3:0>,1	D<4:0>	D<4:0>			
WrReg	0110_0110	ID<3:0>,0	A<8:4>	A<3:0>,D<15>	D<14:10>	D<9:5>	D<4:0>
WrPixel	0110_1001	ID<3:0>,D<15>	D<14:10>	D<9:5>	D<4:0>		
RdReg	0110_0110	ID<3:0>,0	A<8:4>	A<3:0>,0			
Sync	1000_0001_0111_1110						

Carte FE pour quad



1 stave = 13 modules

(modules : 6x 4 chips)

(quad)

50 Core par colonne

8x8 Pixel Core

Digital Chip Bottom

Radiations 1GRad

FPGA

ASIC or in the FE concentrator

LPGBT

Optical converter

Optic fibre

Speed reducer

10 (or 20) Gb/s

~ 40 m

Down link

160 Mb/s

control

Sortie Aurora

Up link

1.2 Gb/s

(programmable ; ÷ 1, 2, 4, 8, 16)

Erreur $<10^{-12}$

2-bit

Down link (stave)

4.2 Gb/s

Experiment

Protocol communication : les symboles

4 groupes : <Sync>, <Trigger>, <Command>, <Data>

Symbol	Byte 1	Byte 2	Comment
Comma	10000001	01111110	for synchronization
idle	10101010	= byte 1	no command or trigger
T0001	11010001	= byte 1	single triggers
T0010	11010010	= byte 1	
T0100	11010100	= byte 1	
T1000	11011000	= byte 1	
T1001	10011001	= byte 1	double triggers
T1010	10011010	= byte 1	
T1100	10011100	= byte 1	
T0101	10010101	= byte 1	
T0110	10010110	= byte 1	
T0011	10010011	= byte 1	
T0111	10000011	= byte 1	triple triggers
T1011	10001011	= byte 1	
T1101	10001101	= byte 1	
T1110	10001110	= byte 1	
T1111	11001100	= byte 1	quad trigger
C1	10101001	= byte 1	standard commands
C2	10101100	= byte 1	
C3	10100101	= byte 1	
C4	10100110	= byte 1	
C5	10100011	= byte 1	
C6	10110001	= byte 1	
C7	10110010	= byte 1	
C8	10110100	= byte 1	
C9	10111000	= byte 1	
Payload data	01a$\bar{a}$bb$\bar{c}$c$\bar{c}$	01d$\bar{d}$e$\bar{e}$f$\bar{f}$	

15

→ S$\bar{S}$ (6 x « 0 » or 6 x « 1 » ; le max)

(1 trame de synchro toutes les 32 trames)

Les T interrompent les data streams

Les T couvrent 4 BCO

dont calibration

Configurations 34 bits
Erreurs 16 bits
Warning 16 bits
Monitoring 16 bits

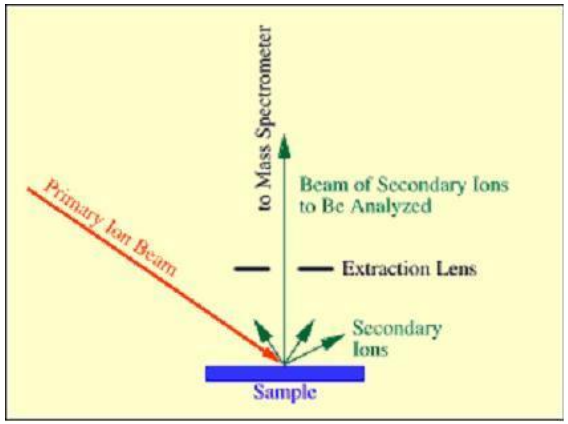
Data utiles (sortie) 32 bits

Profiles de dopages pour calibrer les simulateurs

Deux méthodes experimentales

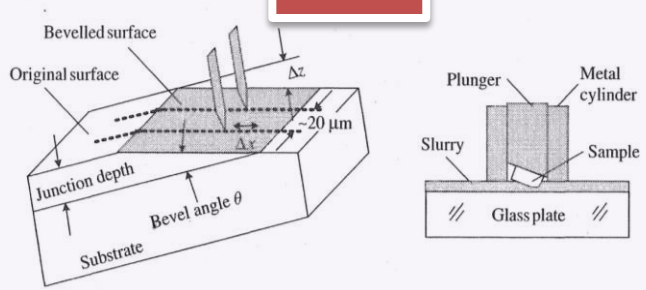
- Secondary Ion Mass Spectrometry (SIMS) – GEMaC – CNRS
  (concentration de dopants [at.cm^{-3}] vs profondeur [nm])
  - Spreading Resistance Profiling (SRP) – EAG metrology lab, U.K.
    (concentration porteurs actifs [cm^{-3}] vs profondeur [nm])

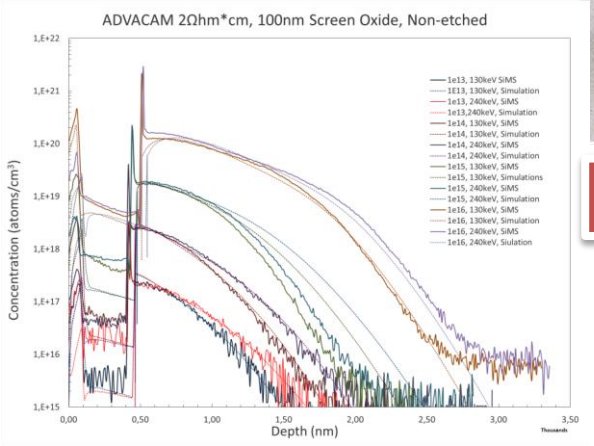
RD50 : Radiation hard semiconductor devices for very high luminosity colliders



SIMS

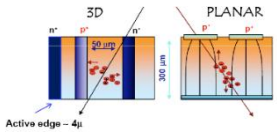
SRP



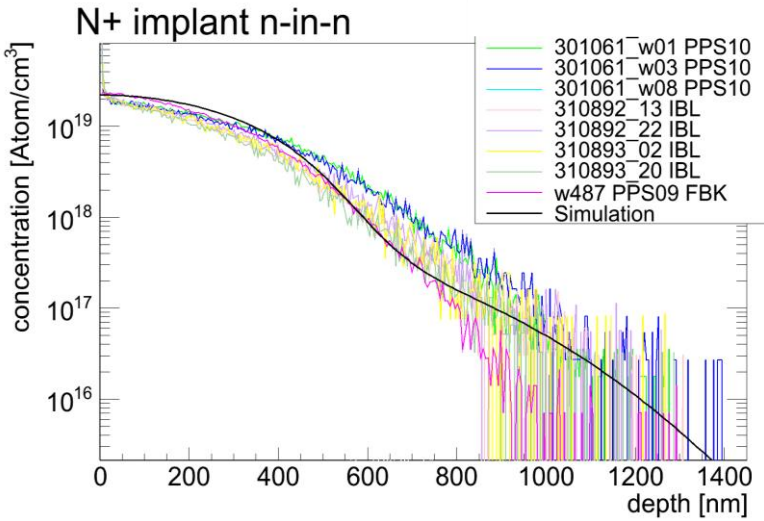


Compare with (3D) **TCAD** simulation for VTT

(R&D)



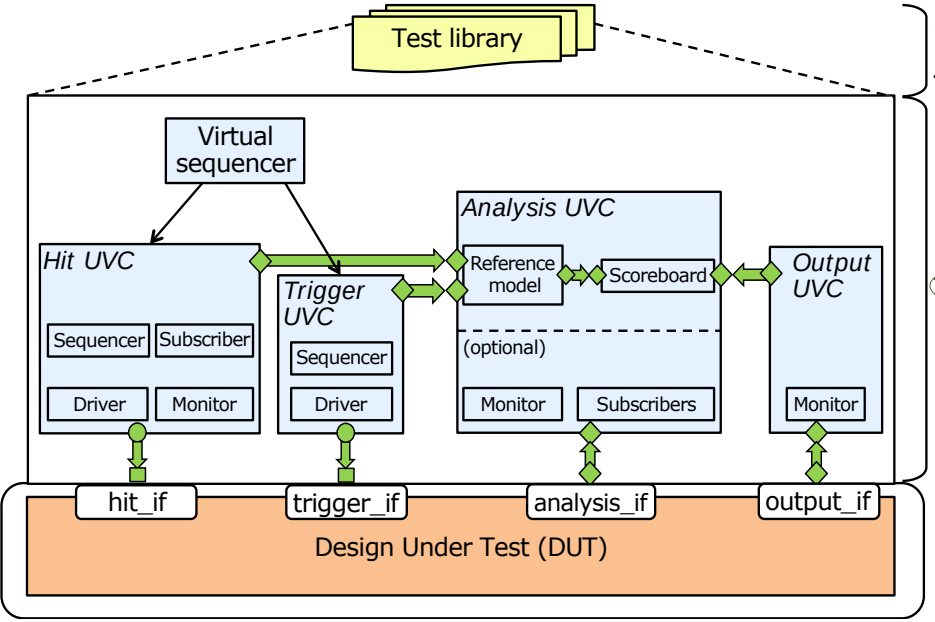
- «LGAD »



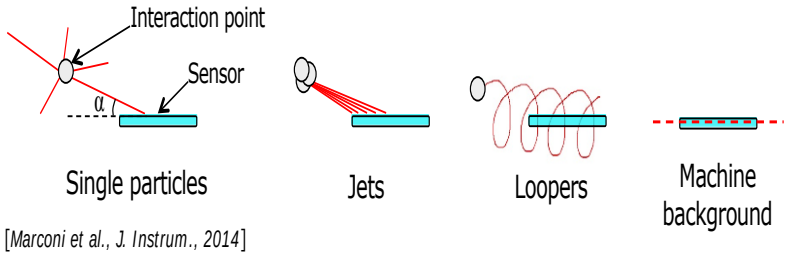
Universal Verification Methodology (UVM)

VEPIX53: ***V****erification* ***E****nvironment for RD****53 PIX****el chips*

(SystemVerilog/*available: git.cern.ch/reps/VEPIX53*)



TEST SCENARIO



[Marconi et al., J. Instrum., 2014]

TESTBENCH

- hit generation and injection
- monitoring of pixel chip input and output
- conformity checks and statistics collection
- S.E.U.

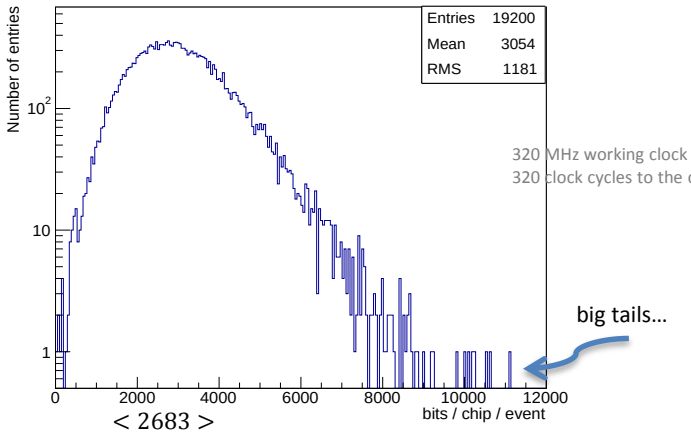
TOP MODULE

Hit : ~ 2 GHz/cm2

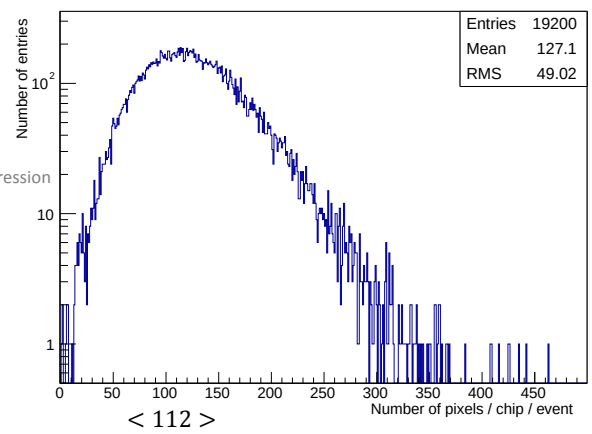
Readout rate (~ 4.8 Gbits/s per chip for 1MHz L1 trigger rate)

Number of active pixels per chip per event

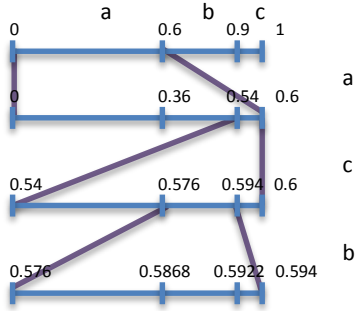
(No compression)



(Compression)



Arithmetic compression :



Cahier des charges ATLAS-ITk-Pixel-FE

Sensor, hit rate, tigger

Spécification	Valeur	commentaire
Sensor thickness	150 µm	
Passivation	non	HV sur les bords ?
Courant d'entré	négatif	Max avant dommages ? (high dE/dx , beam loss, …)
MIP [électrons]	~ 12 000 (théorique)	↘ (Small pixel et irradiation) **(÷2)**
Peak de Landau (MIP)	2 000 e-	Après irradiation (50 % de perte) (RD43A)
Discharge	100 ns / MIP	
Pileup	**≤1%** (≡ return to baseline <400ns)	Hit still discharging, 10ke$^-$, 2GHz/cm^2
Occupancy	0.2% par pixel	par BC à 3 Ghz/cm^2
Capacité	100 - 200 fF	Edge x2
Courant de fuite (après irradiation)	10 - 20nA	(and Edge x2)
Pixel size	50x50 µm^2	
Hit rate nominal	500 MHz/cm^2	
Hit rate Max	1-2 GHz/cm^2 ≡ 0.15%/pixel/BC	4 cm^{2}x 1.5 GHz/cm^2 x B bits, where B is the number of bits per hit pixel needed to store.
Hit loss	≤1% analog (<=0.1% digital)	
Hit loss total	<1% (efficacité 99%)	<3 GHz/cm^2>, 1MHz trigger, 10µs latency
Max hit loss	< 0.1%	**<75kHz/cm^2 >,** 1MHz trigger, **10µs** latency
Recovery après un fort signal	< 1µs	typique

(Technical Requirements / Specifications for the ATLAS ITk Pixel Front-End 5FE Chip ; maurice g s)

Cahier des charges ATLAS-ITk-Pixel-FE

Front End

Spécification	Valeur	commentaire
Pixel size	50x50 µm^2	
Dispersion threshold (σ)	40 - 50 e$^-$	(100 max) **tuned**
Threshold fluctuation [rms]	95 e$^-$	Dans le temps
In time Threshold (dans les 25 ns)	**600 e-** (50%) ≡ 50µm de parcours (MIP)	Tuned, **50fF**, (600e- ≡ 99% des particules)
Threshold temps>25ns	1 200 e$^-$	Need time walk compensation or hit recovery
Noise occupancy (pixels bruyants)	10^{-6} ≡ 0.1 noise hit /BC/chip	50 fF load; in a 25 ns interval
ENC total	126 e$^-$	4.75xENC ≡ probabilité 10^{-6} (threshold)
ENC Front End	73 e$^-$	
Résolution mesure charge	≥ 4bit (0.96 eff)	ou 6 bits (0.99 eff) compressés ou 8 bits programmable
ASIC size	~ 2.0 x 2.1 cm^2	
Bump pad opening	12 µm (Ø)	
Interactions	25 ns	~ 200 évènements par BC
Hit time resolution	1 nsec	
L0 trigger / latency	<1 MHz > / 12.5 µs (programmable)	Digital buffering *(pas de tracking)*
Ou (L0+L1) trigger (encodage<200ns) / latency	< 4 MHz> / 20 µs (≤ 30 – 35 ? µs programmable)	Trigger buffer depth = 16
Consecutives trigger L0	≤ 4 dans 5 BCs, ≤ 8 dans 0.5µs, ≤ 128 dans 128µs	En calibration jusqu'à 16 consécutifs

IN2P3 Institut National de Physique Nucléaire et de Physique des Particules

Consommation et Résistance aux irradiations

Spécification	Valeur	commentaire
400 x 384 chip curent	1.4 A ?	max 2A
Puissance	0.5-0.7 W/cm^2 (1.2V – max 1.32V)	analog 4 µA/pixel, digital 4µA/pixel (max 8 &6)
Température	-40°C to +40°C	
Drift threshold	<5% / °C	
Charge perdue par le sensor	50% (minimum signal = 600e$^-$)	Après radiation
SEU tolerance, data	<0.1% hit data loss	2GHz/cm^2
SEU upset rate, full chip	<0.05/hr	1.5GHz/cm^2, MIP
SEU upset rate, affecting single pixel	<10/s/chip	1.5GHz/cm^2, MIP
Threshold *drift*	<15 e$^-$ / MRad	
Threshold dispersion *drift*	<60 e$^-$ / MRad	rms
ToT *drift*	<2% / MRad	
ToT dispersion *drift*	<0.1 MIP / MRad	rms
SEU tolerance, global config	<1 upset / 1 000 heures	2GHz/cm^2, MIP
SEU tolerance, pixel config	<100 upset / 1 heure	1.5GHz/cm^2, MIP
Total Ionizing Dose	10 MGy 1.5x10^{16} protons eq/cm^2 *1 GRad* /cm^2	Sur 10 ans à -15°C, au moins 500 Mrad (remplacement of layer L0)

Section efficace SEU (TSMC 65nm) σ = 5.0e-14 [cm^2]

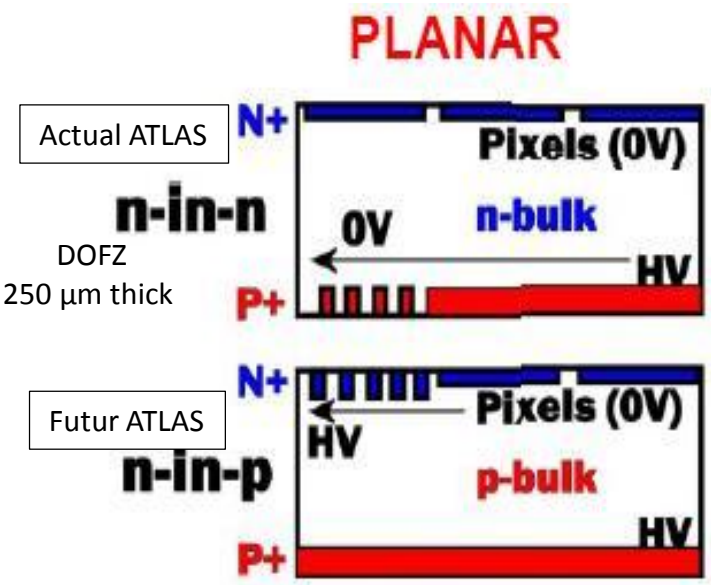
I/O, Timing, fonctionnement

Spécification	Valeur	commentaire
Configuration débit	> 10Mb/s	effectif
Interactions	25 ns	~ 190 évènements par BC
PLL	160 MHz	Stabilité du 40MHz BC ?
Clock skew among pixels	2 ns	Mais ≠ 0
Contrôle interface	160 Mb/s (8 to 10 bit)	série
Output format	CML, SLVDS	70 ou 100 Ω ?
Débit de sortie	5.12 Gb/s	64b/66b protocol : Aurora, GBT, …
Jitter sortie	< 100ps	
Pulse calibration (interne et externe)	500e^- à 40 ke^-	Résolution 30-40 e^- (jusqu'à 10ke^-)
Registres	Accès lecture /écriture	
HitOr	Coïncidences programmables	Self or specific patterns
Mesures	Assurance Qualité	À investiguer
Rendement	Redondance ↗	Dépend du RD53A
Modes	Self trigger et sans trigger. Self tests (PoR)	
Tests, Self test de la fonctionnalité?	Scan chain	À investiguer
Reset	Fonctions ?, PoR (Ident.)	(-40°C to +40°C)

Anneau de garde

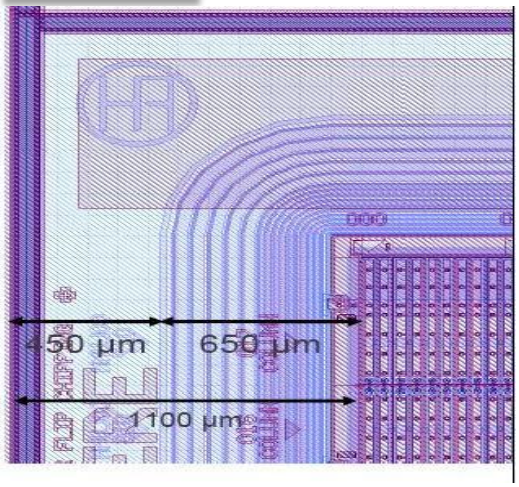
Reduction des zones mortes de détection

modélisation

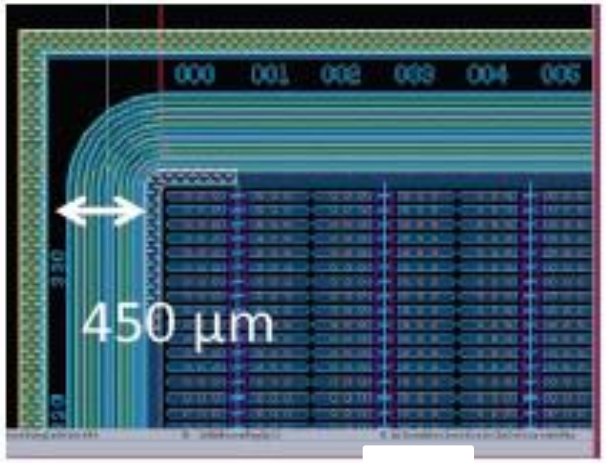


N-in-N

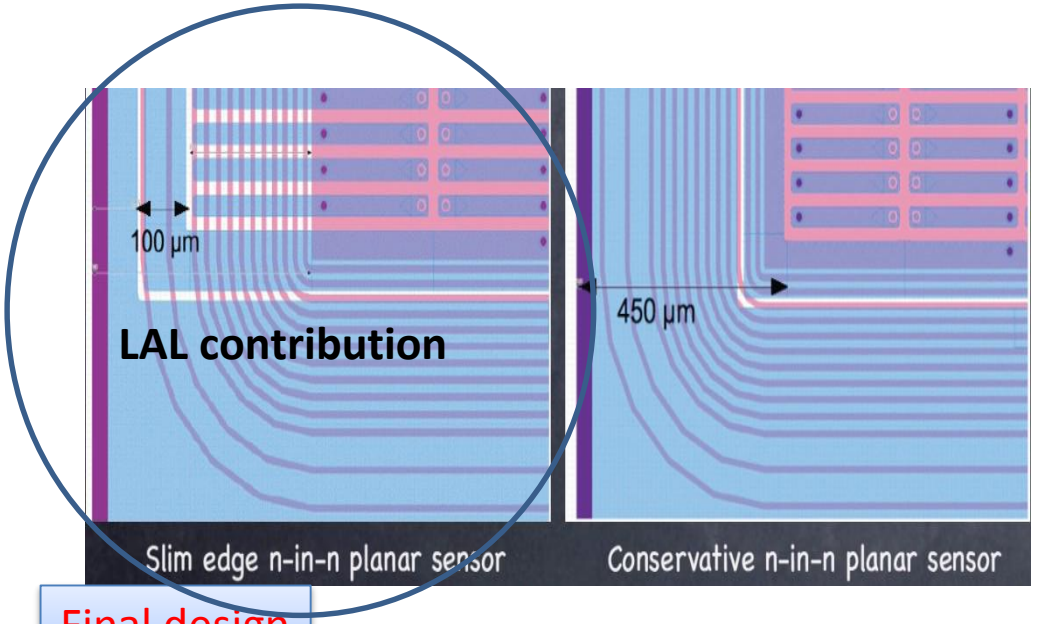
Initial design



N-in-P

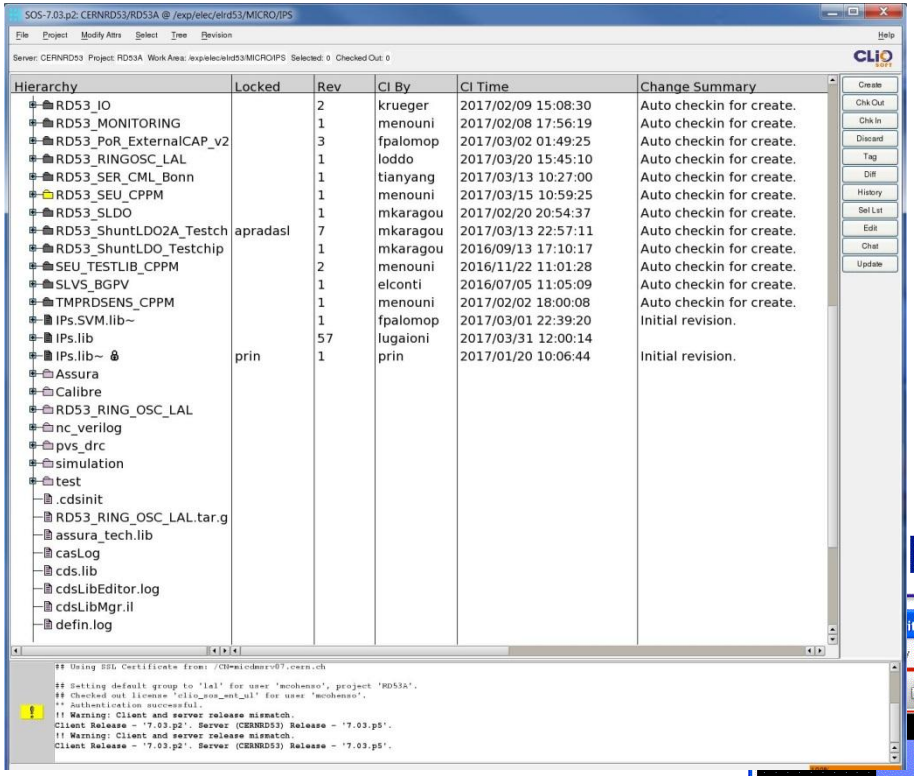


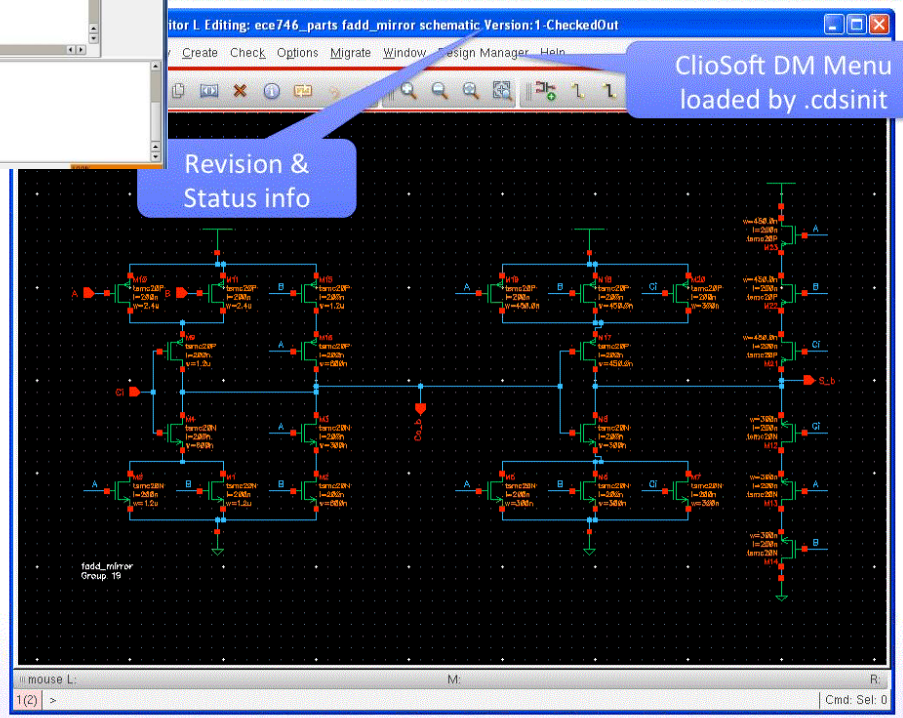
VTT **Edgless** pixel matrix



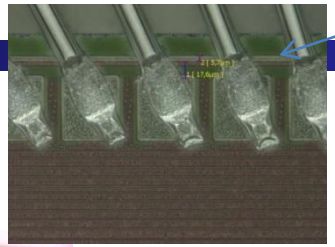
Final design

Editors



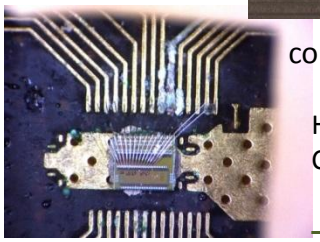


Tests irradiation



Petite carte

- Empreintes
- Connecteurs, câbles
- Buffer/receveur LVDS
- Matériaux (or, alu, chrome, …
- fils

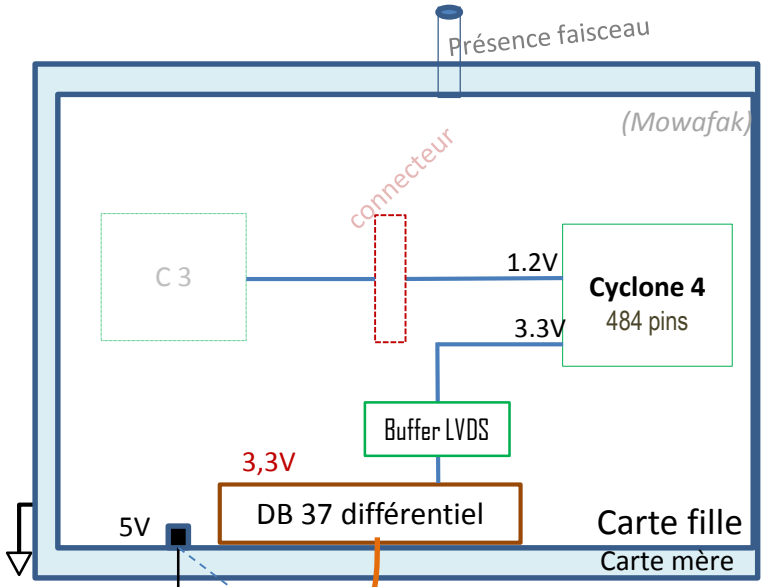


corrosion ☹

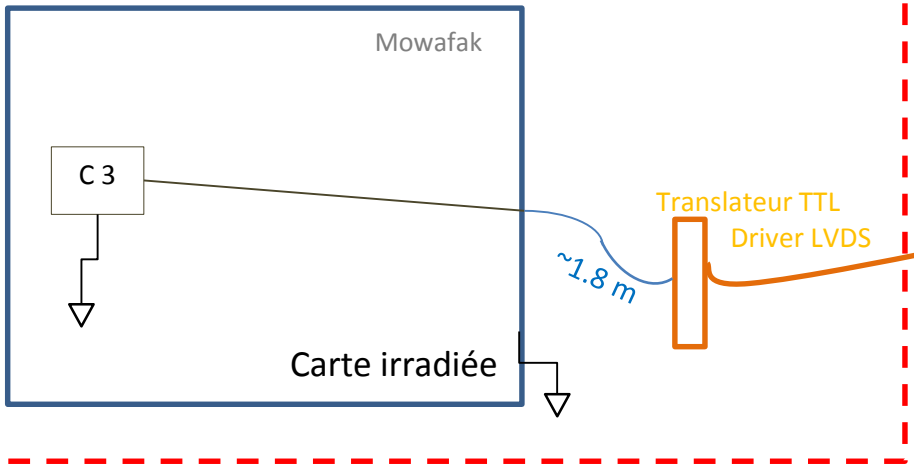
Halogène FR4
Clore , Phosphate, …

→Céramique pure

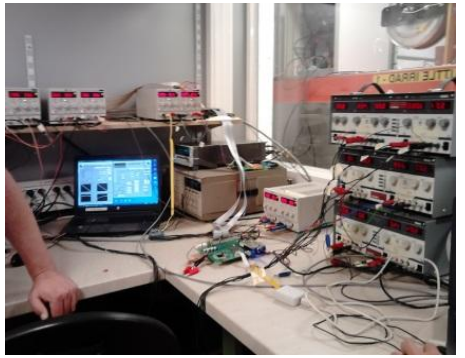
(Set-up, software, formation, suivi médical, accès)



Zone contrôlée

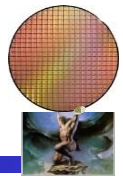


Zone surveillée
(control room)

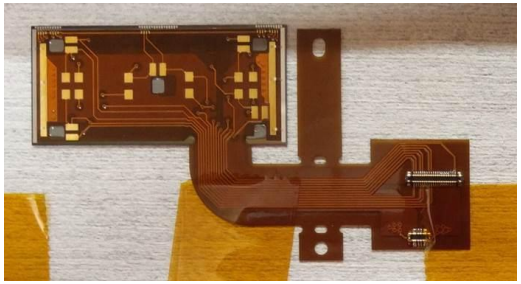


ITk implementation

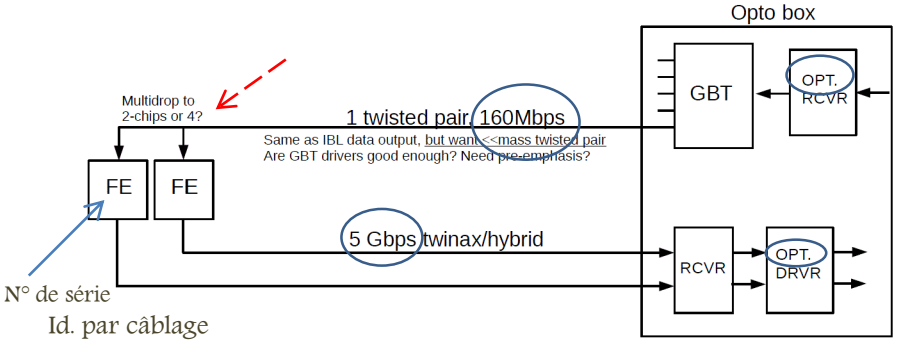
Une amusoire →



Couche interne : still the highest BW

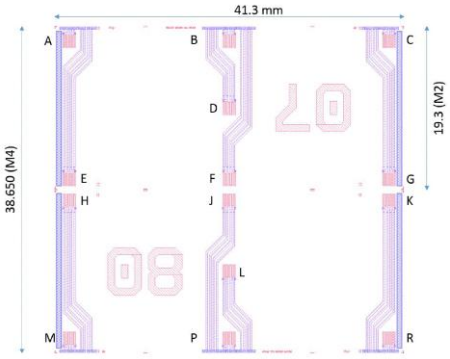


1 module = 1quad



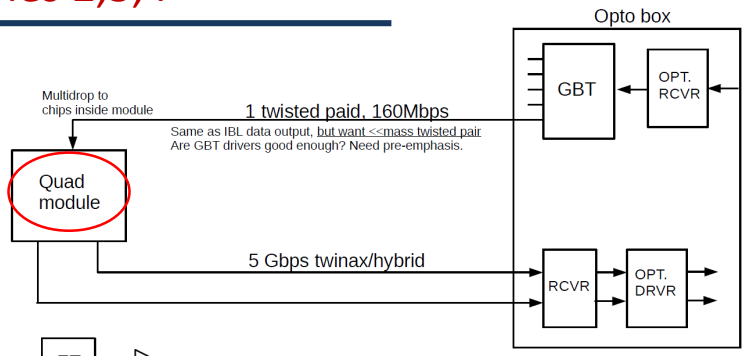
10 000 modules pixel detector

1 échelle (stave) = 78 module ?



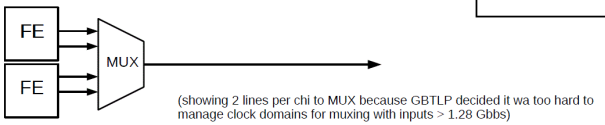
Résistances thermique pour Quad et dual

Couches 2,3,4



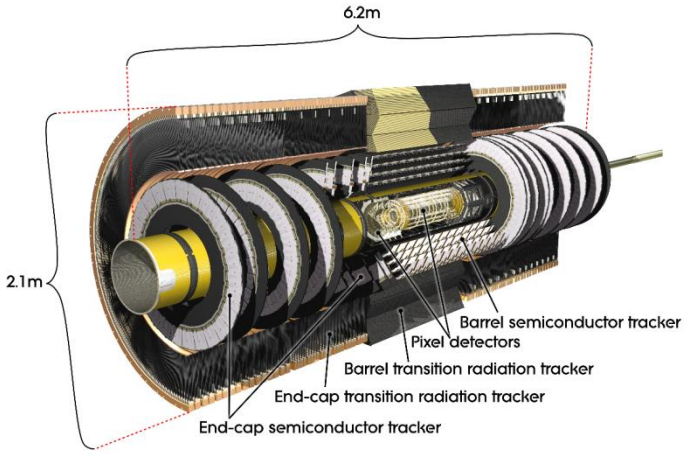
Couches 5

4 FE multiplexés →



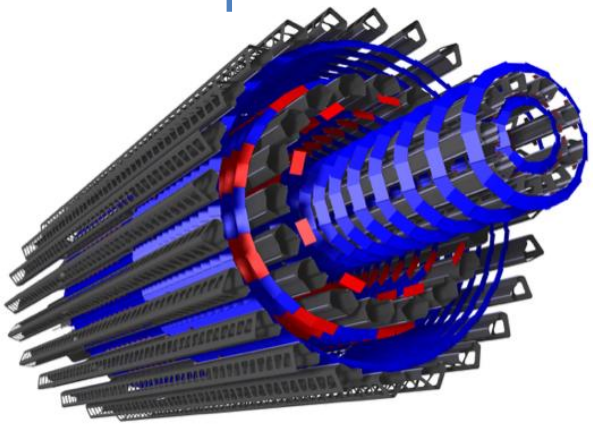
AIDA 2020

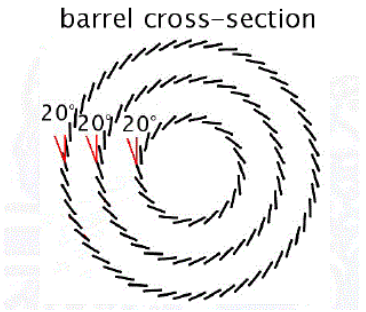
« Inner Tracker »

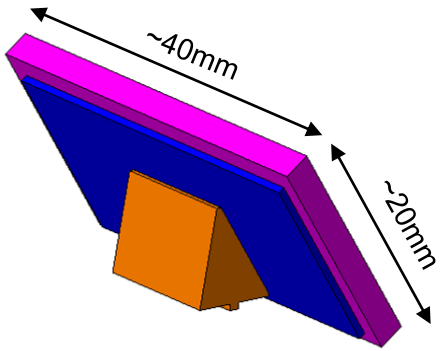


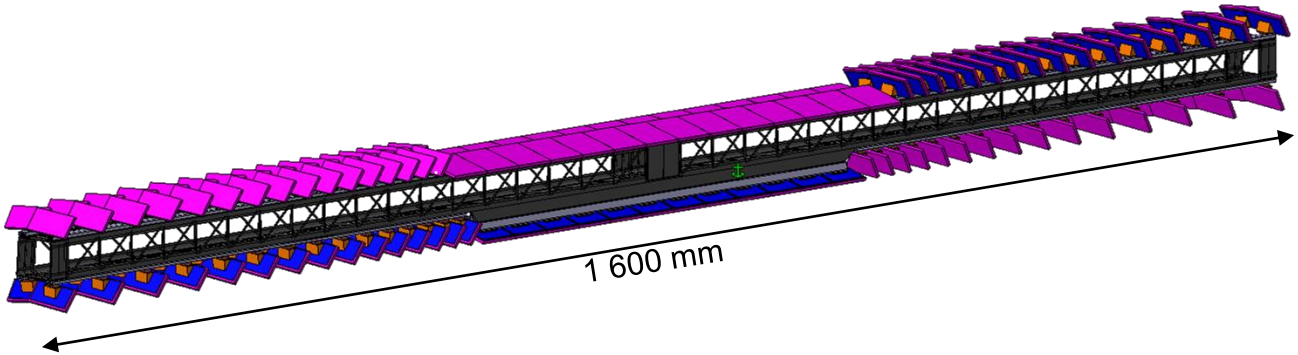
Inner Detector today

Inner Tracker (ITK) in 2025







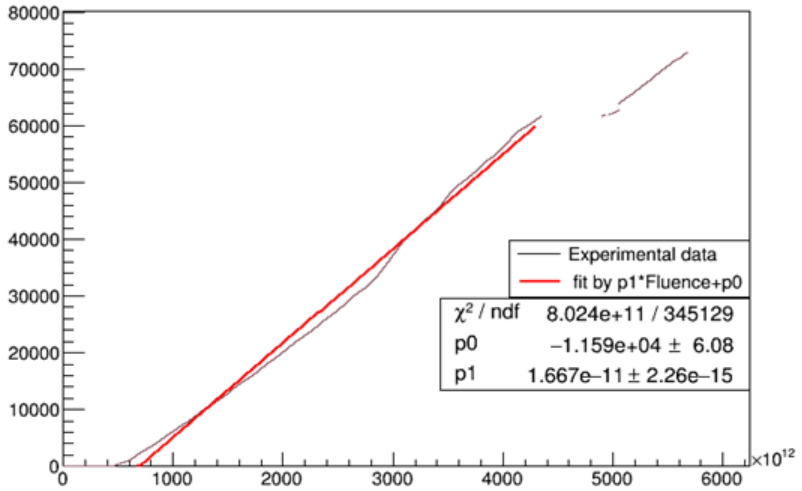


Total errors number vs fluence

8-17 November, not during beam , 2nd Read

Errors

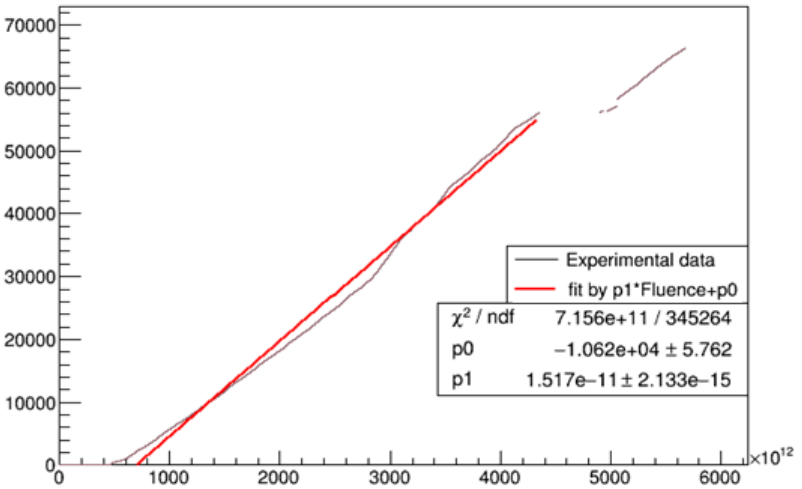
Normal latches



Fluence (p/cm^2)

Errors

Enclosed latches



Fluence (p/cm^2)

Slopes relation

$$\frac{(p1)_{normal}}{(p1)_{enclosed}} = 1.099$$

SEU cross-section estimation

$$\frac{p1}{N_{latches}} \approx \sigma_{SEU}$$

$$\sigma_{normal} \approx 1.54 \times 10^{-14} cm^{-2}$$

$$\sigma_{enclosed} \approx 1.41 \times 10^{-14} cm^{-2}$$

CPPM data

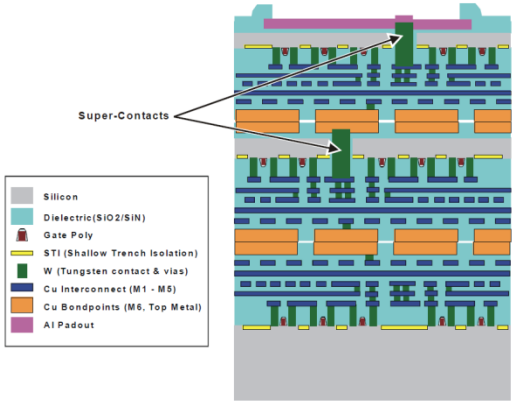
$$\sigma_{standart\ flip-flop} \approx 2.8 \times 10^{-14} cm^{-2}$$

$$\sigma_{normal} \approx 6.2 \times 10^{-15} \mathrm{cm}^{-2}$$

$$\sigma_{enclosed} \approx 5 \times 10^{-15} \mathrm{cm}^{-2}$$

Industry offers **3-D methods**

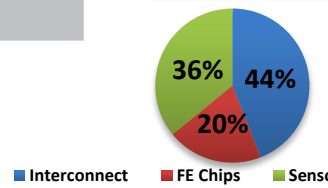
institute	TSV					interconnection			wafer size
	diameter	aspect ratio/depth	filling	pitch	type	type	pitch	diameter	
CEA Leti	30µm 40µm 60µm	1.5:1 03:01 02:01	Cu liner	80µm	from backside to M1	solder pillar (Cu- SnAg) solder bumps (Cu SnAg)	50µm 120µm	25µm 80µm	200/300 mm for TSV?
CMP/MOSIS	100µm	2.5:1 (250 µm)	Cu liner?	400µm	via middle with 0.35 µm CMOS				
EMFT	2 µm 10 µm	> 8:1 4:1 (40µm)	Tungsten Tungsten/C	4µm 20 µm	apect ration: 16:1	SLID (SnCu)	< 30 µm	25 µm	20
IZM	15 µm large (100µm?)	50 µm	Cu filling Cu lining	30 µm large tapered (>100 µm?)	interposer	SnAg(Cu), CuSn, Au, In Au nano porous	20 µm?	10µm	
IMEC	25µm 5µm	2:1 (50µm) 4:1 (20µm)	Cu filling Cu filling	40µm 10µm	via last via middle (with 130nm in-housewe CMOS)	CuSn (in)	20µm (10µm?)		
VTT	60µm (top)	2:1 (120µm)	Cu lining	90µm	tapered (86deg)	SnPb, InSn, PbSn, SnAg	25µm	50µm	
T-Micro	0.5-2.8 µm (tapered) 2.5 µm	< 40µm < 55 µm	tungsten polysilicon	~10 µm small	via last via first	microbumps + adhesive	5µm	2µm	

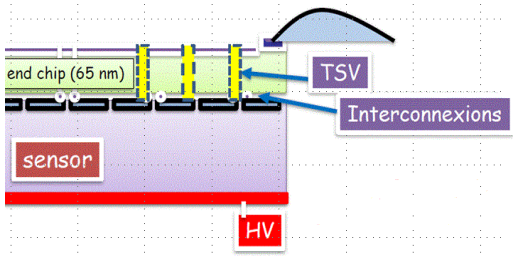


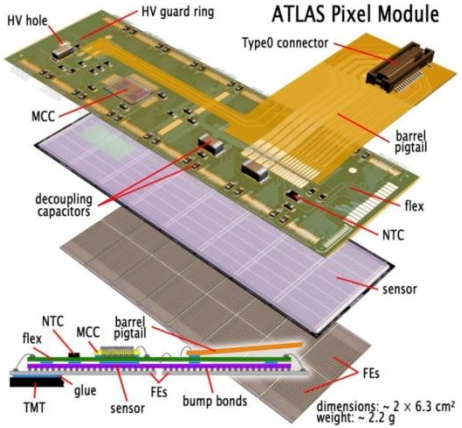
AIDA 2020

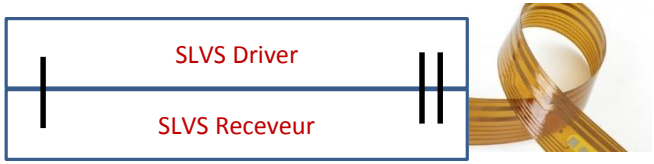
European project

- 4 side abuttable devices
- Shrink pixel
  - Pas de wire bonds (fragile)
  - Pas de bump bonds
- **Rapidité** I/O
- Consommation I/O
- **Coût (réduction 40%)**

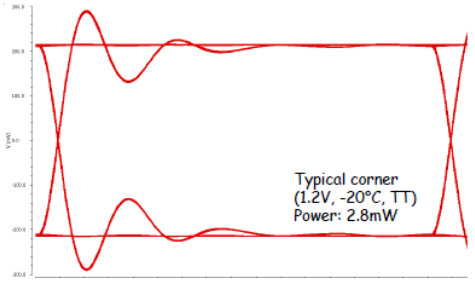








Driver load: CLC (0.5 pF, 1nH, 1pF) and 100 Ω termination resistance

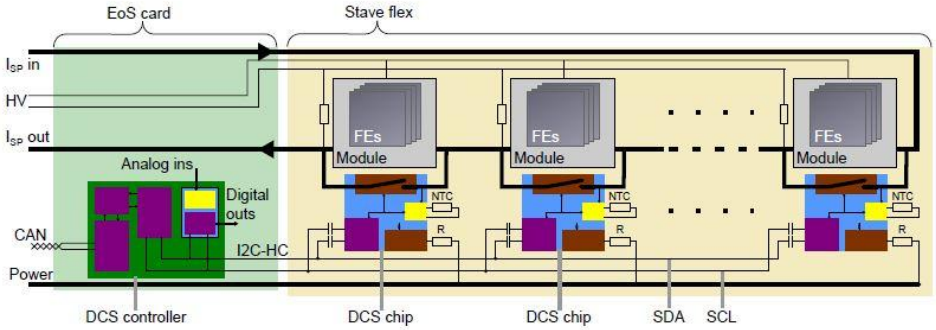


Bandwidth [GHz]	2.3
Rise Time [ps]	83

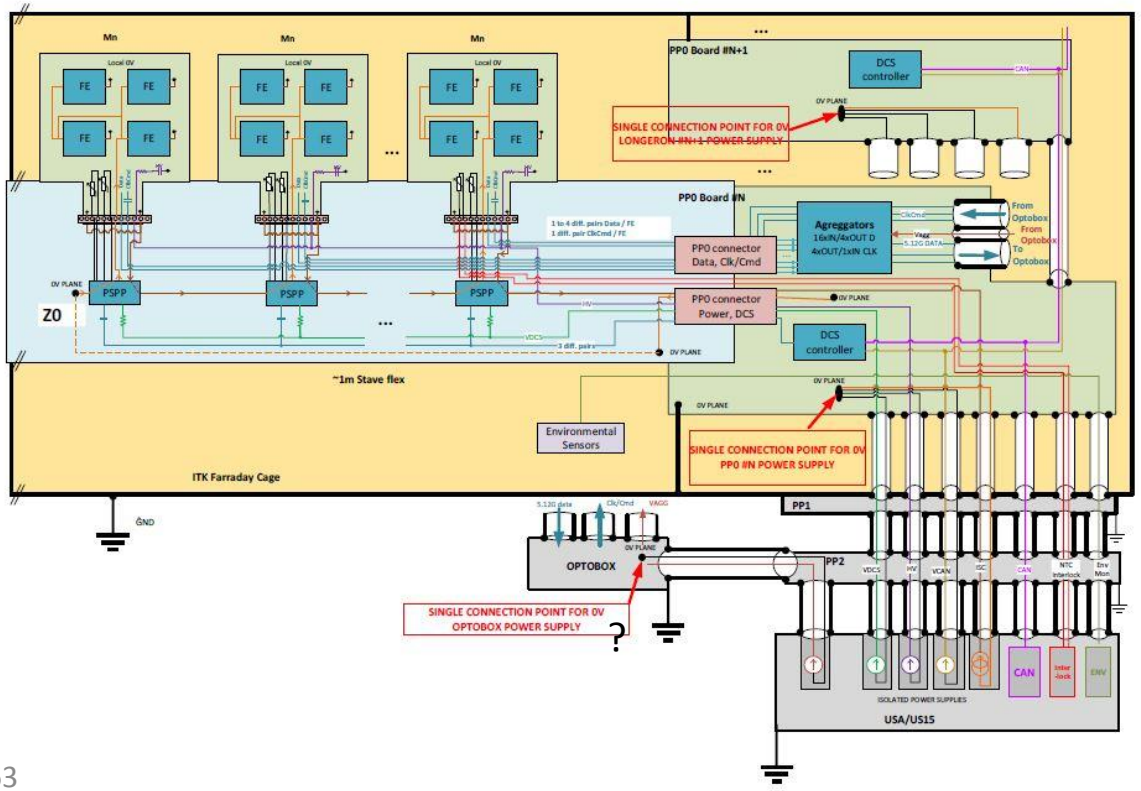
Instead of wire bonding, TSV could be considered in 65nm technology in chip periphery for improved the time transit. *(Collaboration with the CEA LETI-Grenoble)*

Services staves

DCS Concept



Sketch of the DCS components on a half stave.



Technologies

Omegapix_1 130 nm Chartered Semiconductor
64 x 24 pixels, pas : 50µm x 50 µm

Omegapix_2 (3D) **130 nm Global Foundries**
96 x 24 pixels, pas : 35µm x 200 µm

FE-I3 (2003) 250 nm IBM
18 x 160 pixels, pas : 50µm x 400 µm

FE-I4-B (2011) 130 nm IBM
80 x 336 pixels, pas : 50µm x 250 µm

RD53-A (2016) 65 nm TSMC
400 x 200 pixels pas : 50µm x 50 µm