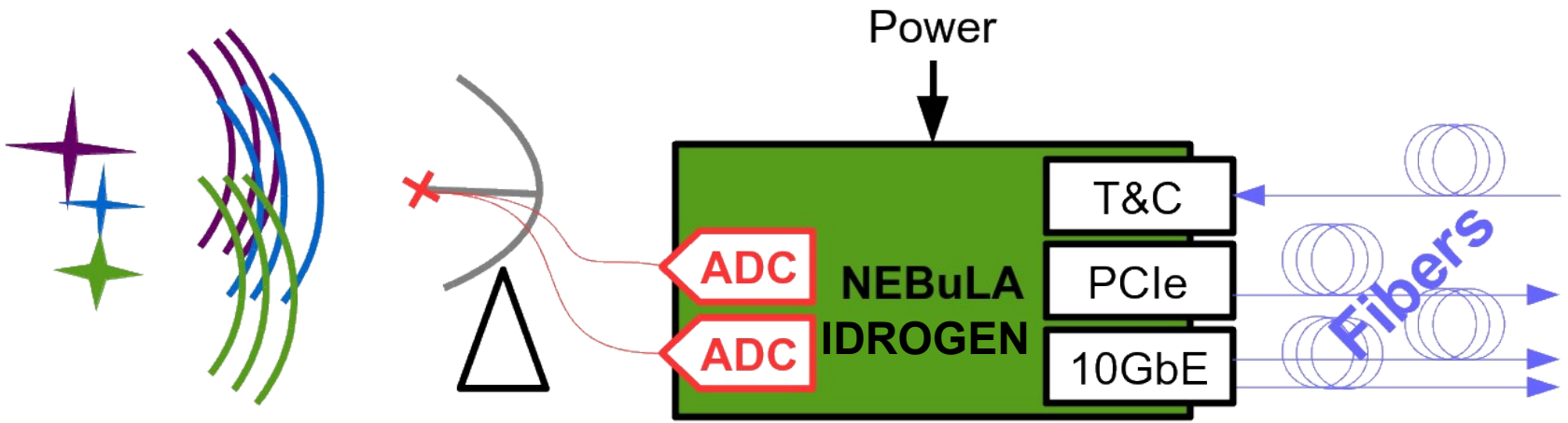
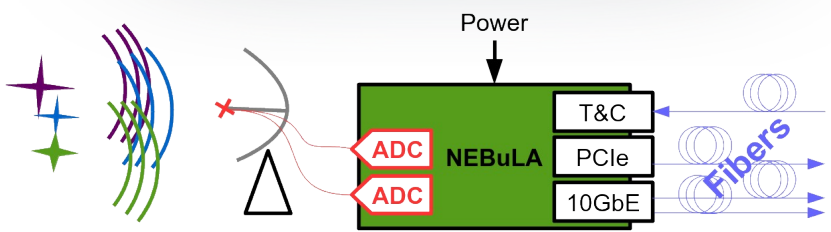
IDROGEN
Digitization board

Cedric Viou[1]
Daniel Charlet[2]
On behalf of the NEBuLA / IDROGEN / DAQGEN developers



1 Station de radioastronomie de Nançay, Observatoire de Paris, CNRS/INSU
2 LAL, CNRS/IN2P3

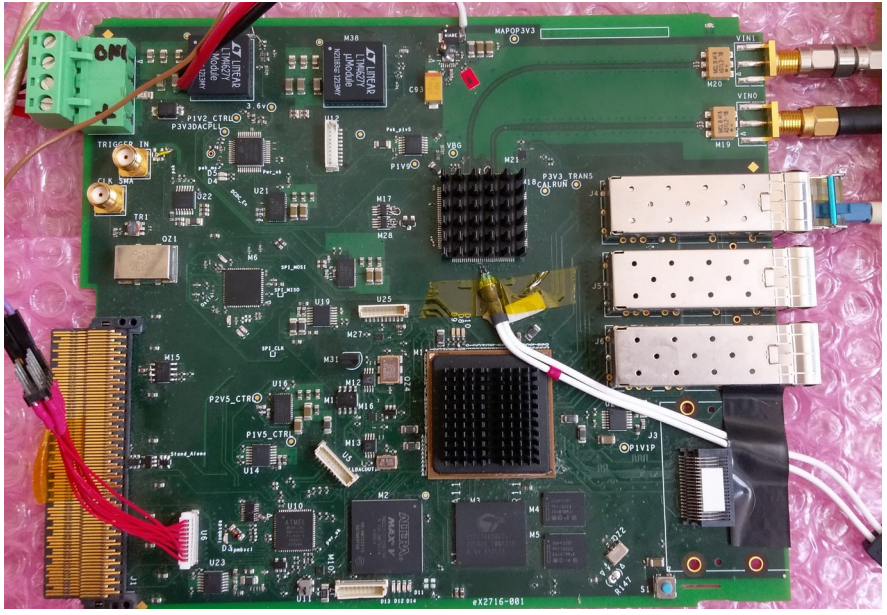


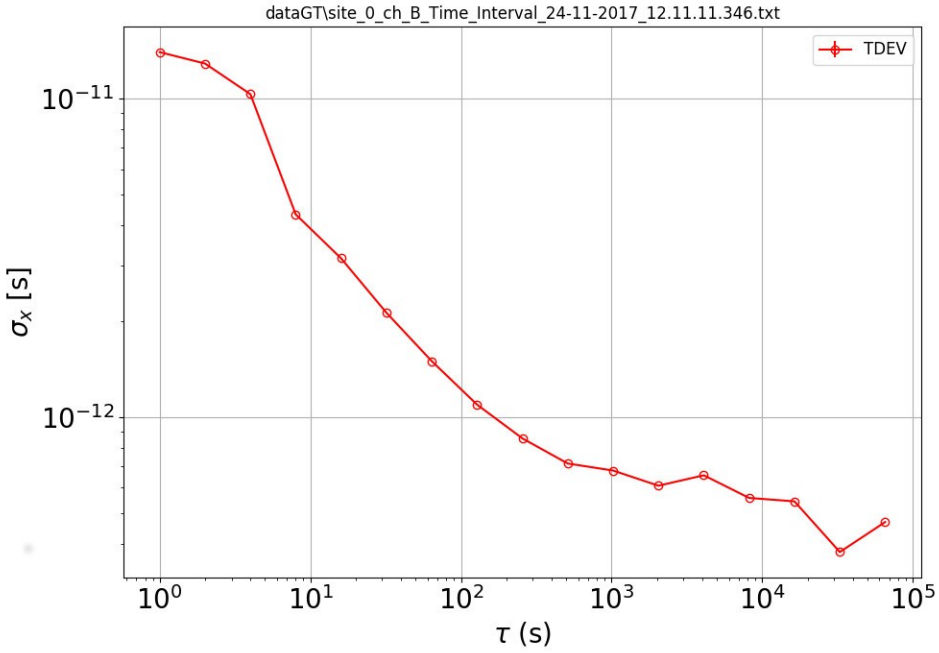
- Historic
- DAQGEN, overview of the architecture
- IDROGEN
  - Hardware
    - Overall Synoptic
    - Clock trees
    - Components configuration
    - Hardware status
  - Firmware
    - Firmware status
  - Software
    - PCIe
    - Slow control
  - Documentation
- Mezzanine ADC

This board took advantage from the experience and know-how of different laboratories from IN2P3 :

- USB-blaster II from PCIe40 board: CPPM Marseilles
- IPMI : LPSC Grenoble
- IPbus: LPSC Grenoble (https://ipbus.web.cern.ch/ipbus/)
- Cadence IN2P3 CAD library: IPHC Strasbourg
- WhiteRabbit module from NEBuLA digitizer:
  - LAL + Nançay (Observatoire de Paris, CNRS/INSU)

IDROGEN / DACGEN History

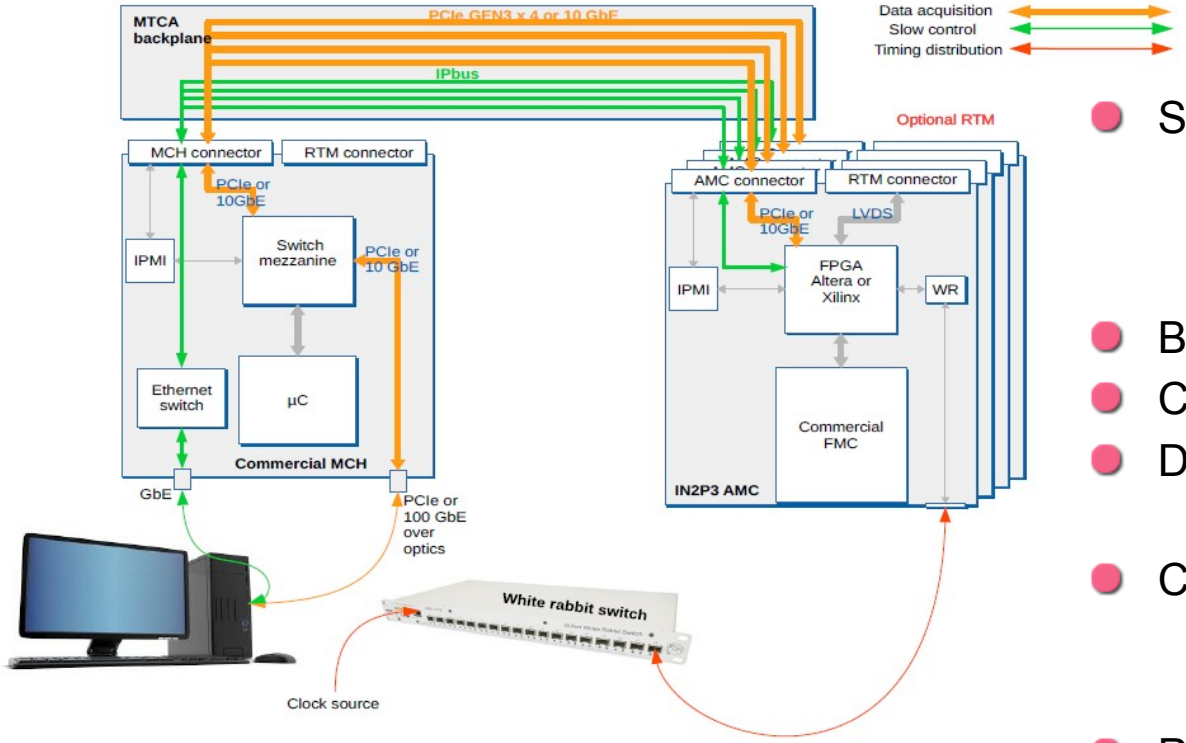




- Derived from Nebula board
  - White rabbit module
  - Power supply tree

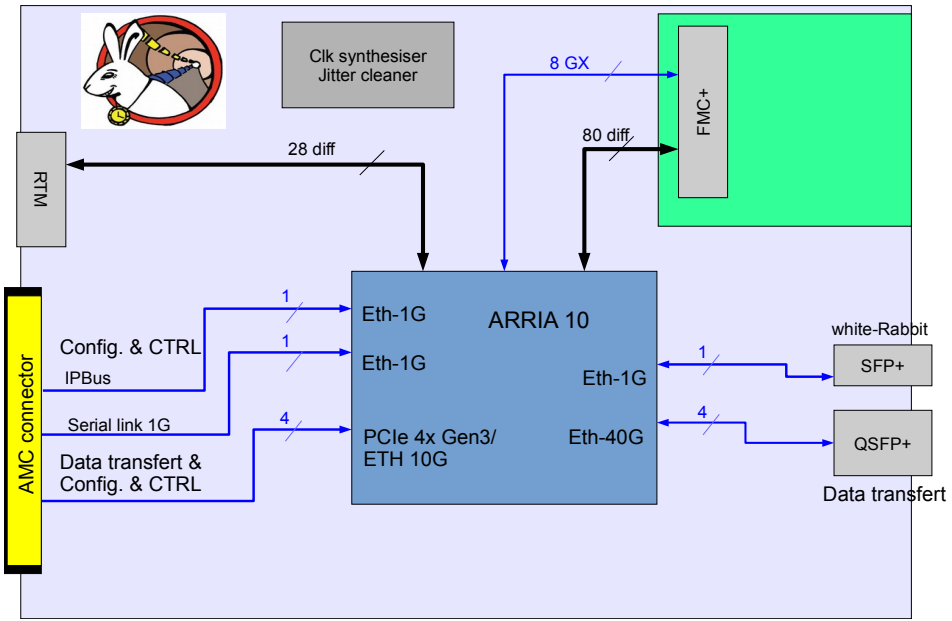
- In collaboration with SYRTE
  - Observatoire de Paris
  - Time-Frequency laboratory
- 400 fs after 1000 s and 1 km fibre

DACGEN: ARCHITECTURE



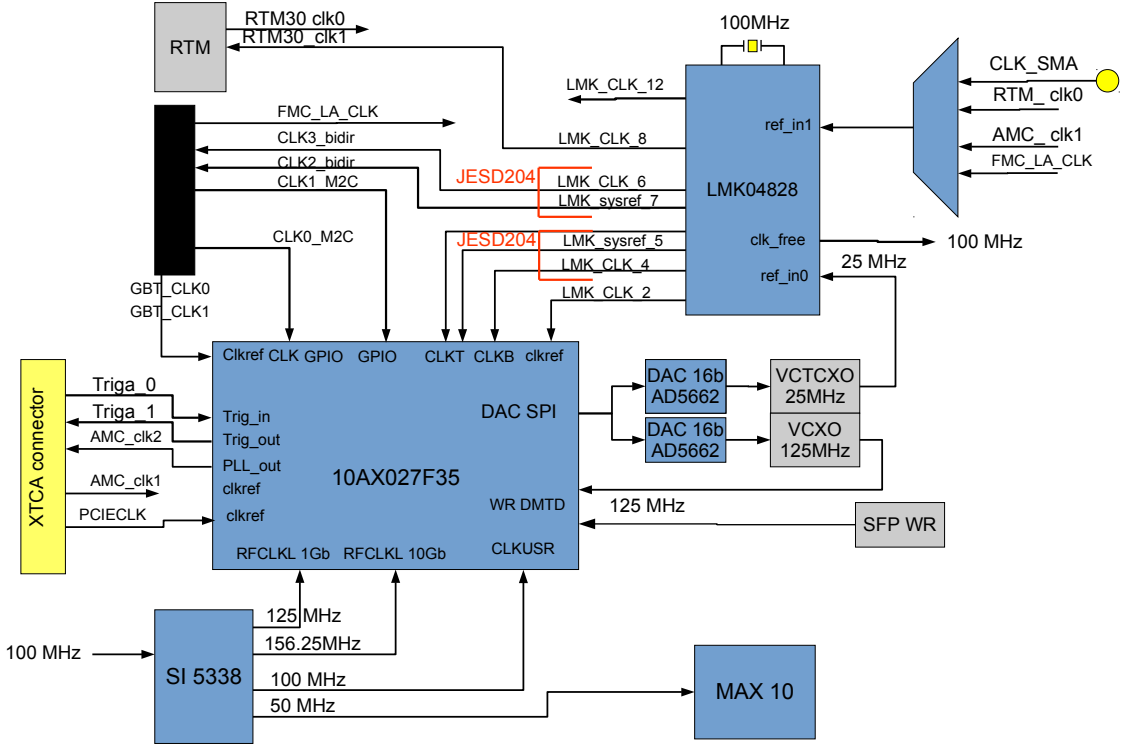
- Standard : xTCA for Physics
  - Faster learning curve for new teams
  - Reference hardware for new and/or existing devels
- Based on on-the-shelf equipments
- Crate controler : MCH from NAT
- Data read-out on backplane :
  - PCIe 4x Gen3 ou 10GbE.
- Crate data transfer :
  - PCIe-over cable (industrial NAT)
  - 100GbE (industrial NAT)
- Point to point Data read-out
  - 2x10GbE
  - 40GbE (future development)
- Board configuration : IPbus

IDROGEN board main feature



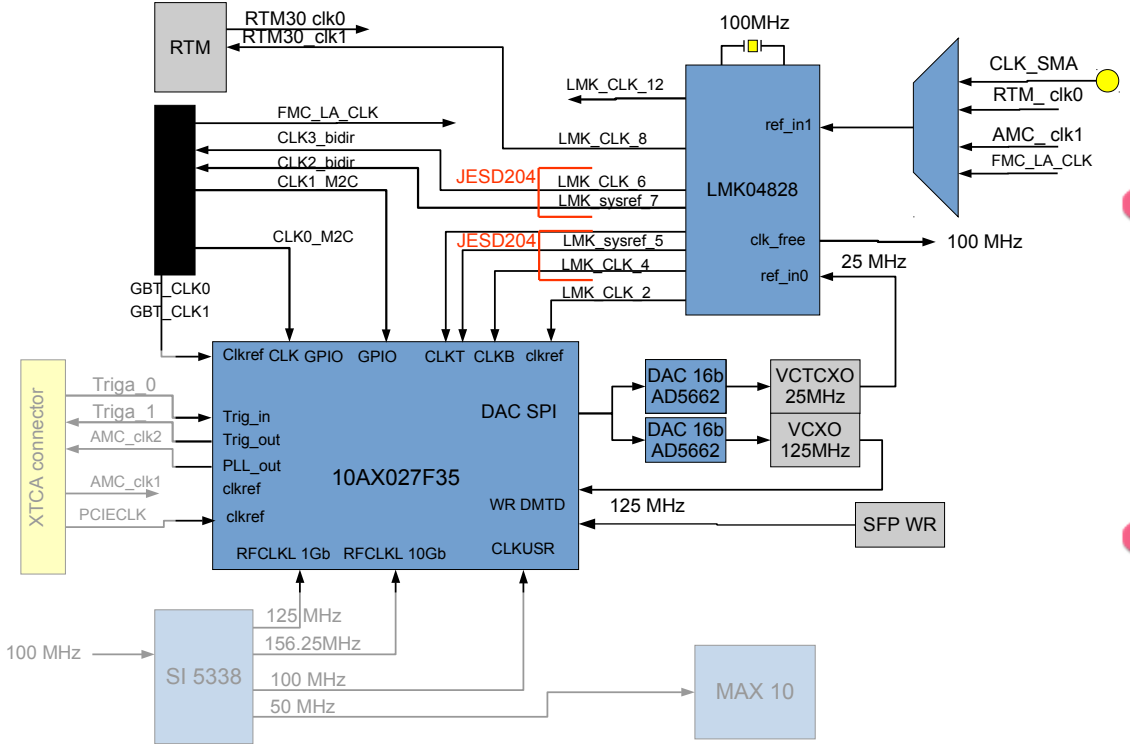
- MTCA 4.0 standard, Double-width, full size AMC.
- FPGA : Intel/Altera 10GX027H4F34
- Stand alone power supply 12V
- VITA57.1 (FMC) slot.
  - 160 single-ended I/Os (80 LVDS) and/or up to 10 serial transceivers in a 40 x 10 configuration
- White Rabbit compliant.
- Front panel connectivity :
  - WR SFP+
  - QSFP+ 40G, USB
- Backplane connectivity :
  - 1Gbe IPbus, PCIe Gen3 x4
  - IPMI, CLK & trigger lane.
  - RTM connector : J30.
- Low cost

Clock tree: main features 1



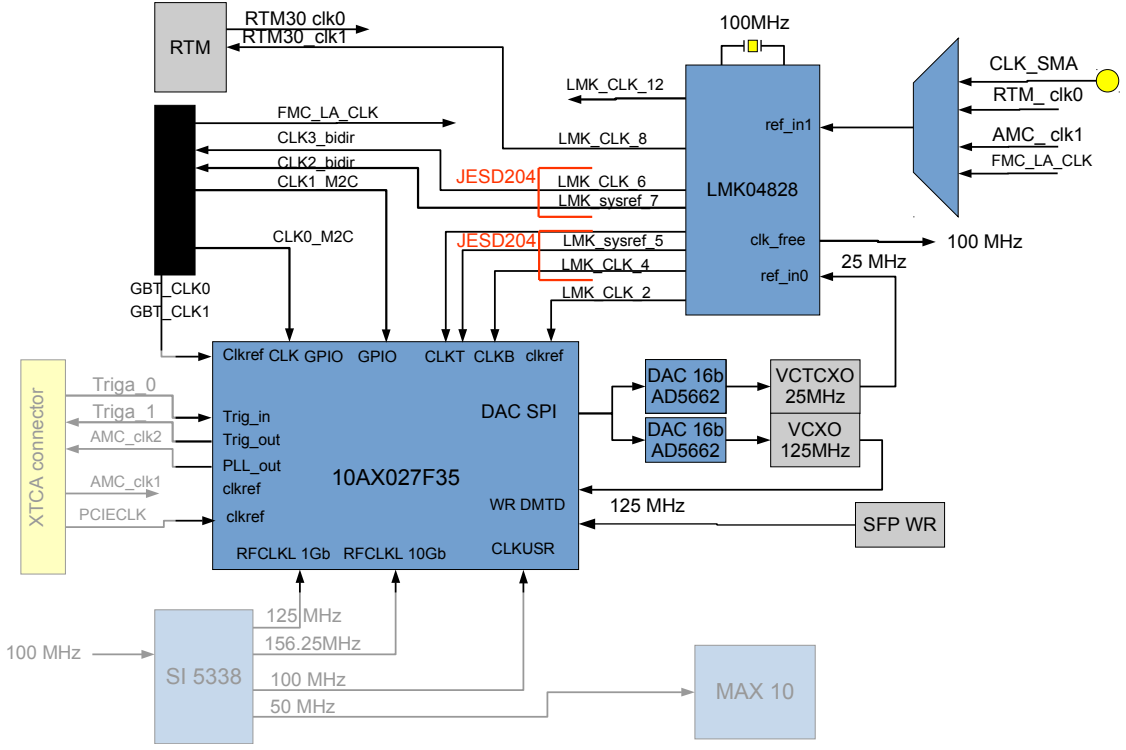
- 2 clocks synthesizers
  - LM04828 jitter-cleaner for RF clocks.
  - SI5338 low-jitter for transceiver ref clocks.
- All clocks on-board derive from synthesisers with single sources.
- All clocks routed in differential.
- Two dedicated JESD204B-compliant clocks
- Configured by µC
- Dedicated tools for configuration.

Clock tree: main features 2



- LMK4828 clock in :
  - White-Rabbit module.
  - SMA connector.
  - RMT30 connector : CLK0.
  - FMC connector : LA_CLK.
  - AMC connector : TCLKB.
- LMK4828 clock out :
  - FMC connector JESD204B compliant : Clk2_bidir, Clk3_bidir .
  - RTM : CLK1
  - FPGA : CLKREF, clk.
  - AMC_CLK2
- FPGA received also direct clocks from different sources :
  - FMC connector
  - AMC connector
  - RTM connector

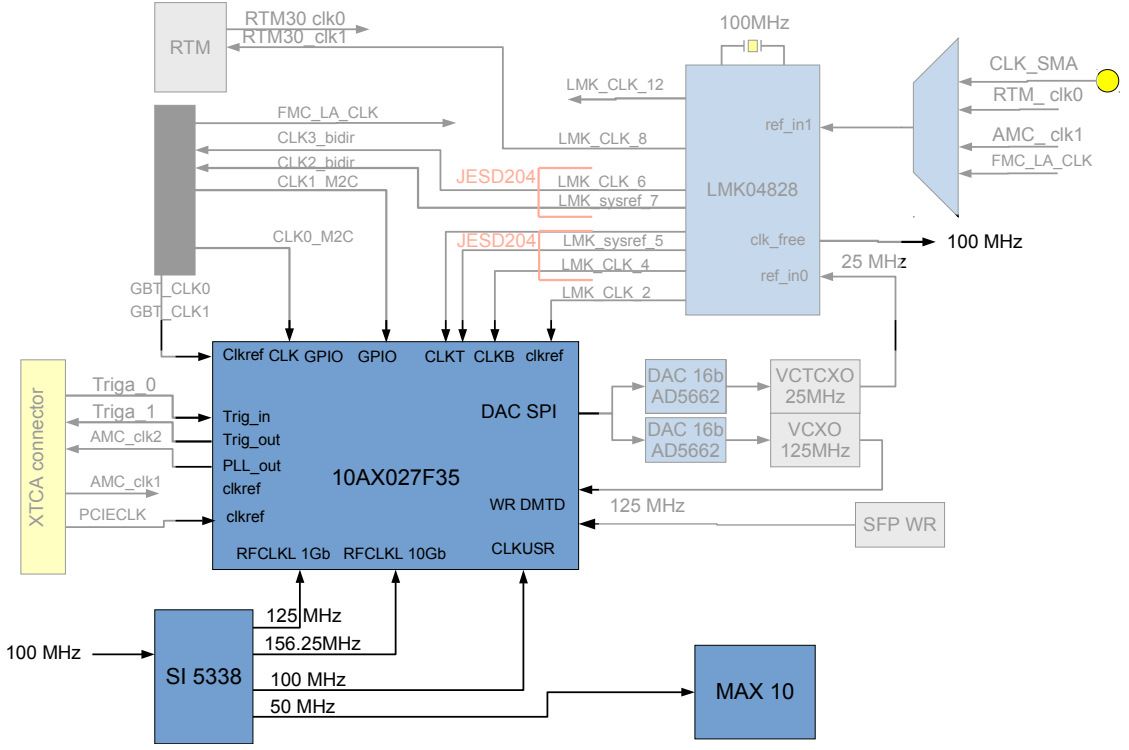
White Rabbit clocks



A improvement of the open hardware design have been done by LAL/Nançay Observatory.

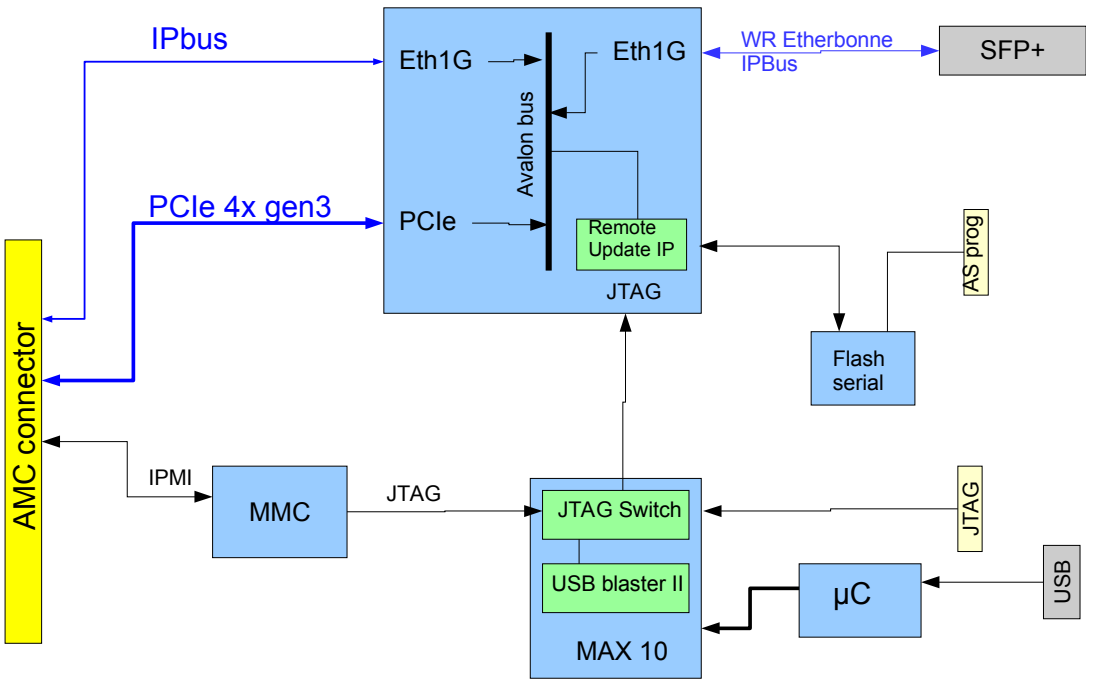
- Based on LMK4828:
  - Ultra low noise clock jitter Cleaner with Dual Loop PLL
  - 90 fs RMS jitter
- Low noise VCXO and ref clock frequency modification
- Dedicated power supply.

Serial protocols clocks (1GbE, 10GbE, 40GbE, PCIe)



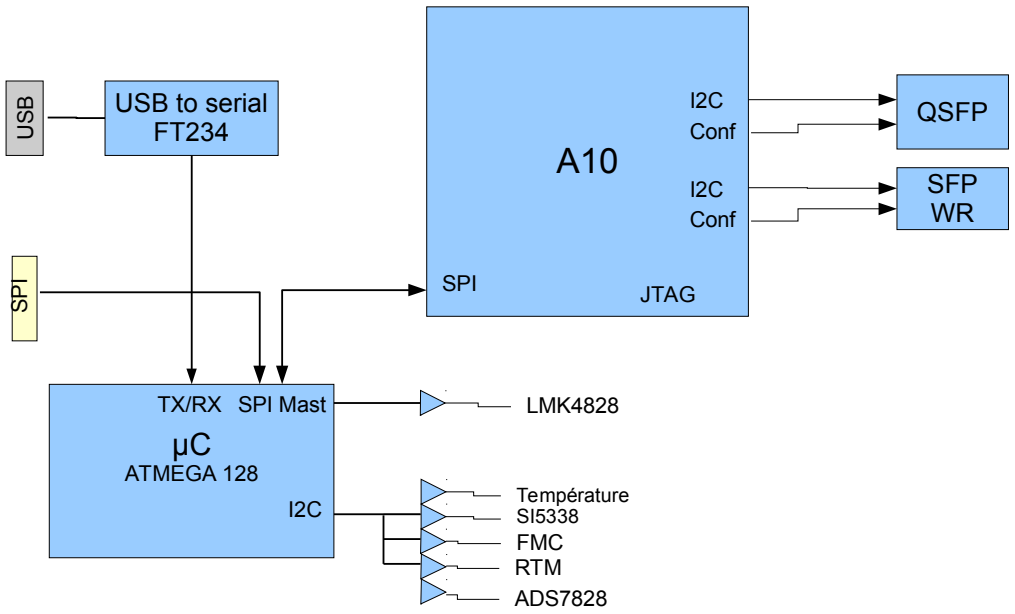
- The serial links clocks are generated by a dedicated synthesiser (SI5338)
  - Configured by µC
  - Input clock reference:
    - LM04828 clk_free
    - “free-running” clock locked on ref_in1
  - Output clock:
    - Refclk AMC ETH0
    - Refclk ETH10G
    - CLKUSER
    - Max10

FPGA configuration



- Three FPGA configurations capabilities :
  - On-board serial Flash (active serial)
    - EPCQL 256kb
  - JTAG
    - On-board USB-blaster II
    - Connector
  - Remote update :
    - IPbus.
    - WhiteRabbit Ethernet link
    - PCIe (optional)

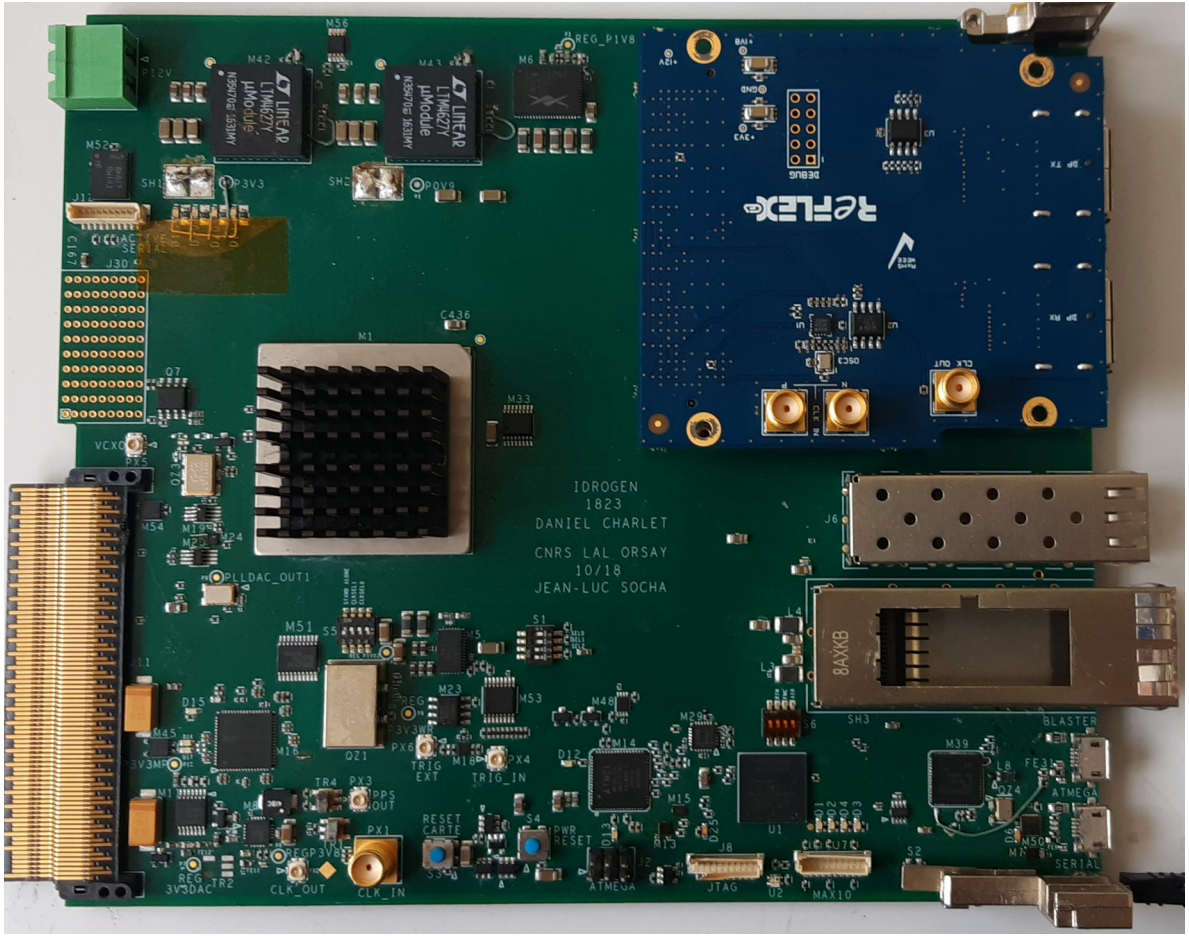
Components configuration.



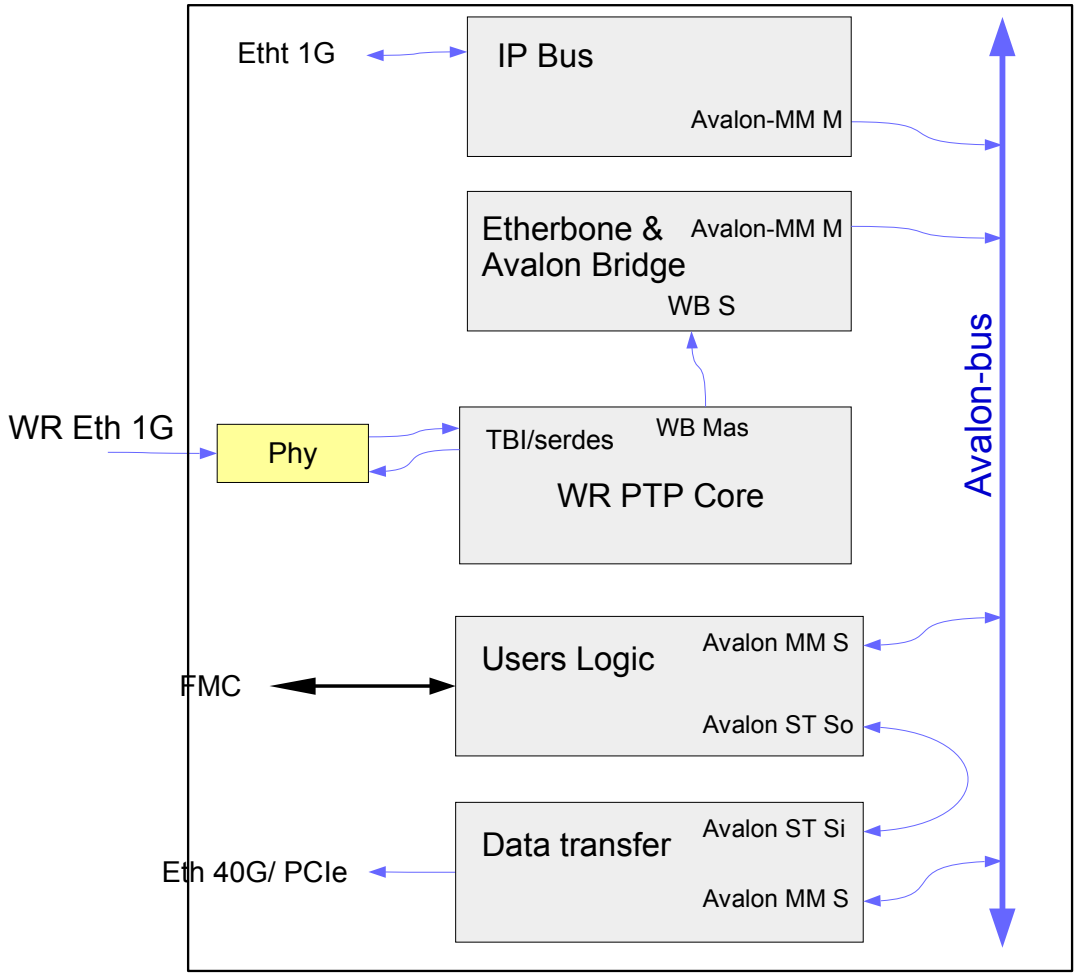
- The mains components are configured by the µC throught I²C and/or SPI.
- The on-board configuration (µC flash) is performed at the power up.
- The configuration could be modify by :
  - USB with dedicated software
  - IPbus or WR through SPI bus (in devel)
- The transceivers are read/configured by the ARRIA10
- µC is configured:
  - SPI dedicated connector.
  - SPI FPGA (not tested).

Hardware Status

- IDROGEN-2 PCB currently in production
  - 2 pre-series board
- Test up to end of 2019
- 10-board production : beginning of February 2020.
  - 5 for PAON IV project (DIMACAV).
  - 1 for CPPM, CENBG (IN2P3)
  - 1 for IPHC (IPHC)
  - 2 for Nançay Observatory
- Delivery of boards : May 2020



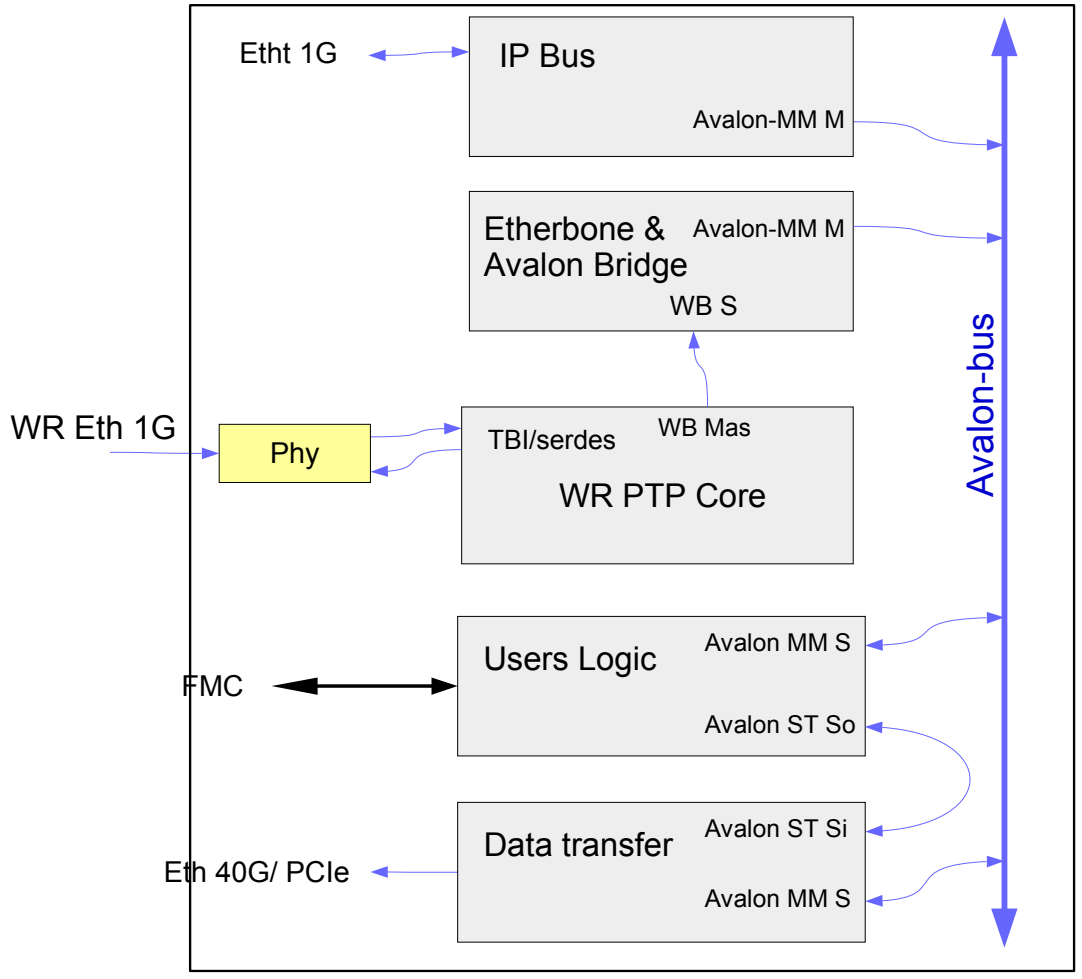
Firmware architecture



The NOC firmware is developed using QSYS (now System Designer)

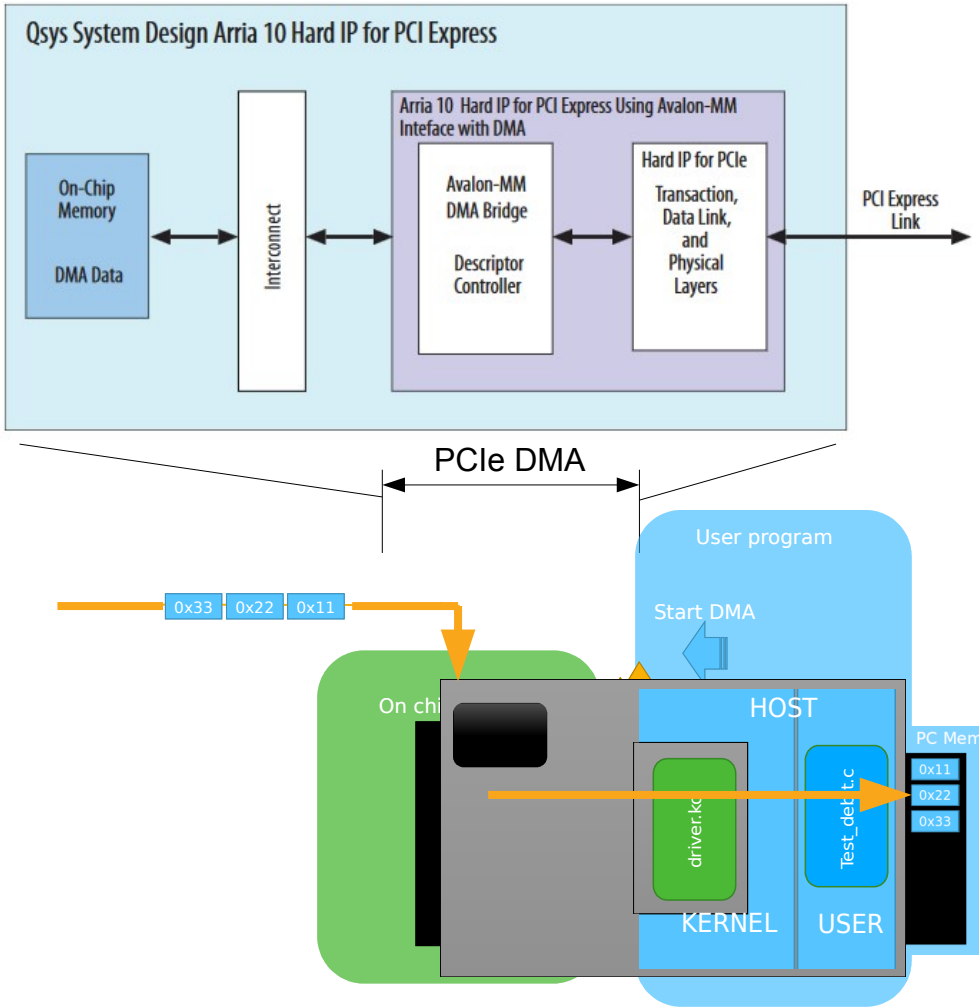
- Two QSYS Avalon master : IPbus & WR
  - WhiteRabbit PTP core, Avalon master bus.
    - Manage all functionalities for the WR
    - Etherbone protocol.
    - Interface to FPGA core by Wishbone to Avalon interface.
  - IPbus, Avalon master bus
    - Slow-control
    - Data read-out
- Users Logic, interface to FMC connector.
    - Avalon Slave interface.
    - Avalon Streaming source to data-transfer module
- Data transfer, data read-out
    - 2 x 10GbE Ethernet
    - PCIe Gen3 x4
    - 40GbE if IP available at IN2P3

Firmware status



- WR PTP core : CERN open-core
  - Tested
- Etherbone & Avalon bridge
  - Tested
- IPbus
  - Ongoing porting at LPSC
- Existing bloc to integrate for data transfer:
  - PHY, MAC : Intel IP
  - UDP framing (CASPER project)
  - ARP (CASPER project)
  - Users Logic :
  - ADC Ref design supplied by Analog-Devices.

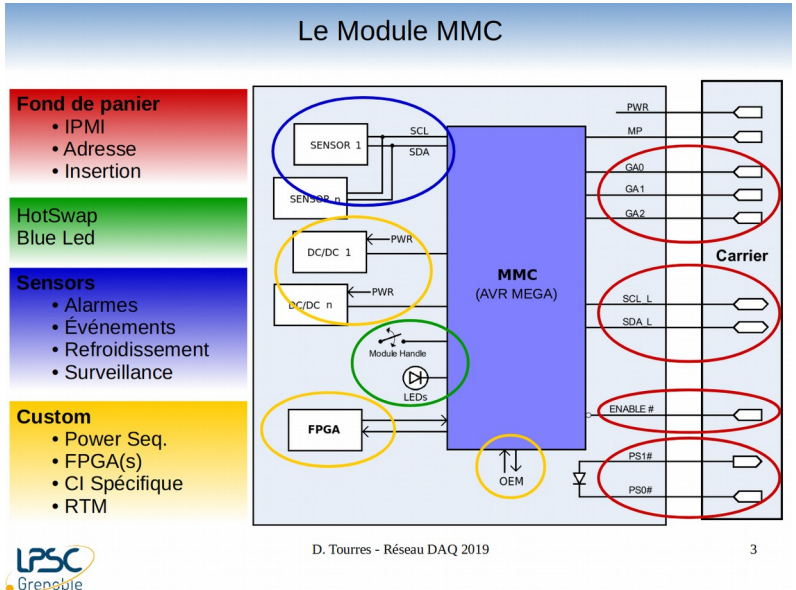
Acquisition Software for IDROGEN (M.Taurigna)

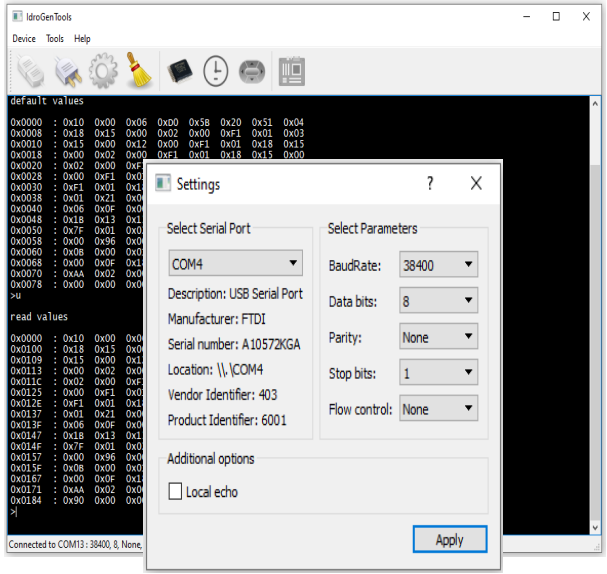


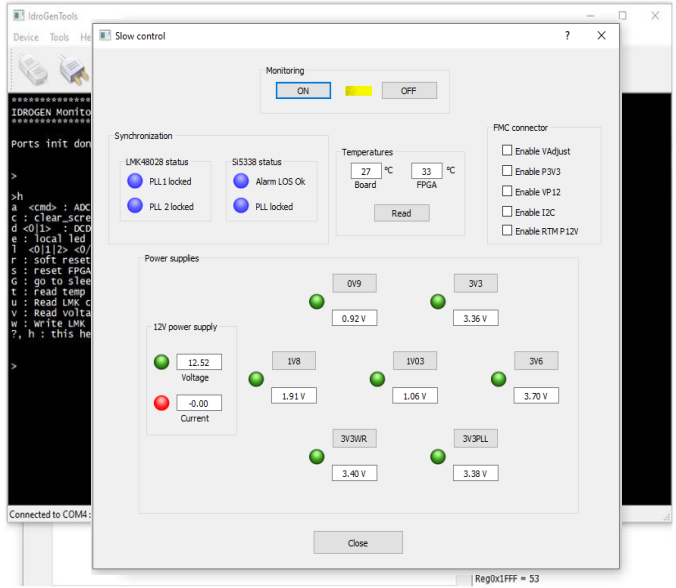
- Intel IP PCIe Avalon-MM-DMA
- DMA transfers require :
  - One (or more) memory buffers allocated in host memory
  - Trigger DMA
    - By host, through register polling
    - By host, through Int (next developement)
    - By application
- Currently developed in the PCIe40 board for CCPM/CERN for LHCb.
- To be transfered to IDROGEN board (same FPGA family)

IDROGEN Slow control

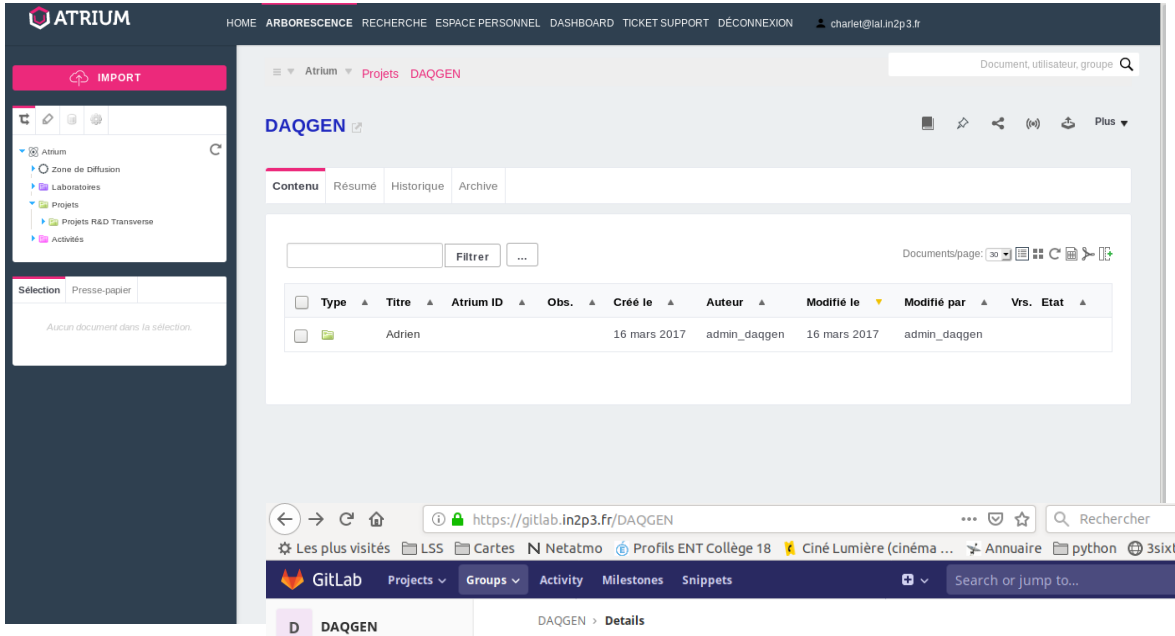
- Based on 2 ends of a software link:
  - **IdrogenMMC**
    - Embeded software running on the ATMega128 of IDROGEN.
    - Based on MMC-DAQGEN library developed at LPSC.
  - **IdrogenTools**
    - Server-side GUI meant to configure and test IDROGEN.
    - C++ / Qt5 App developed for Linux/Windows

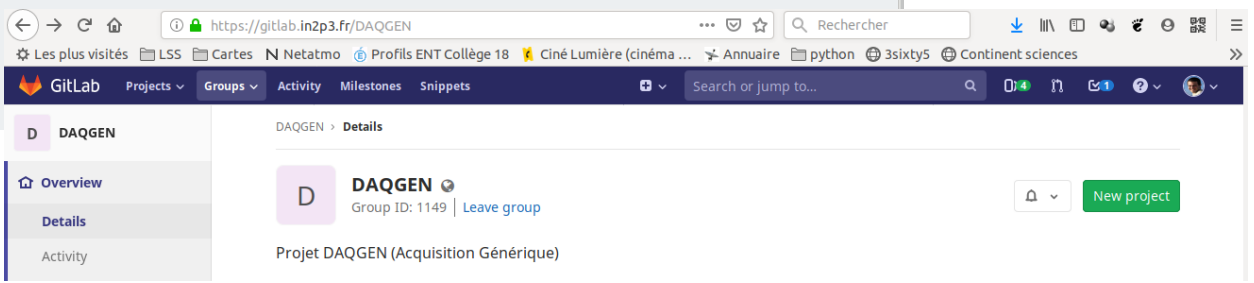






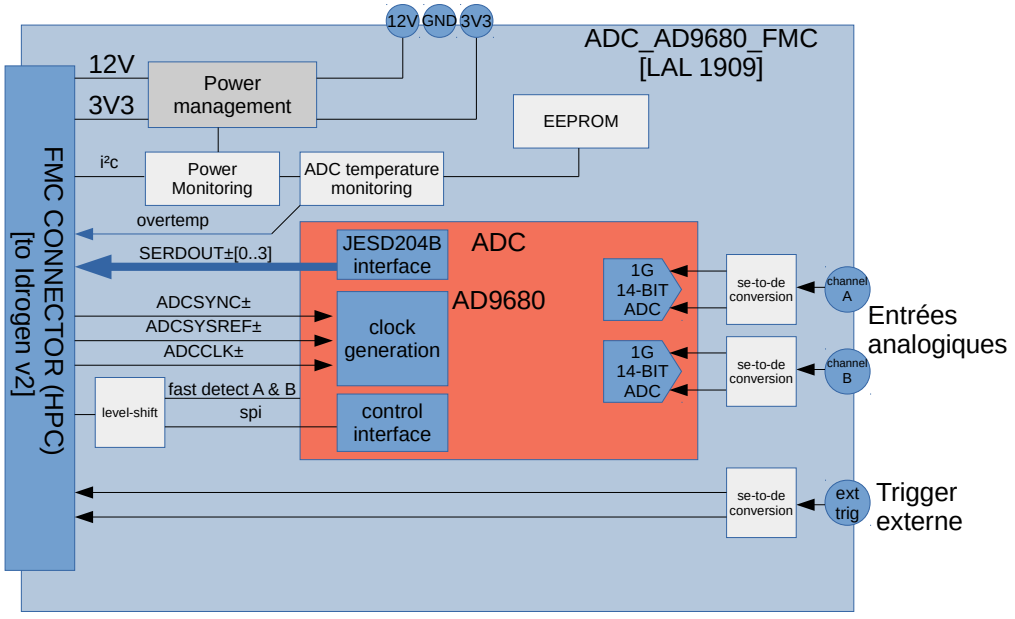
Documentation





- Schematics
- Board Layout
- Firmware
- Software
- Documentation

Mezzanine ADC

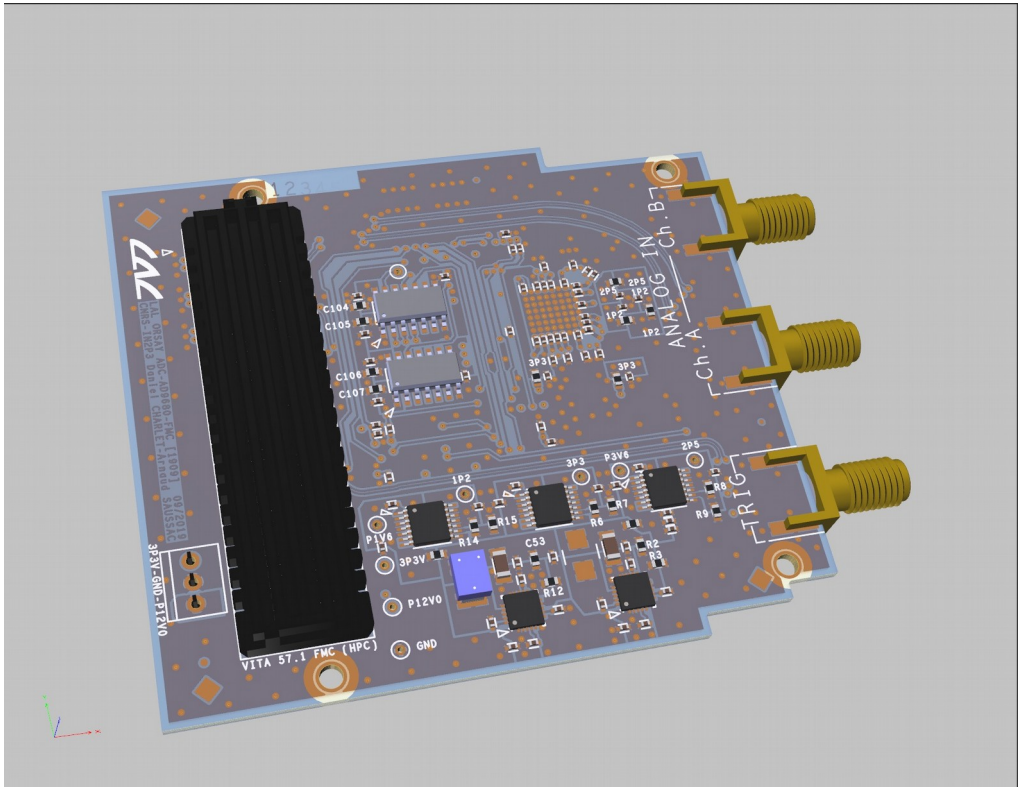


The motivation of the development of a new mezzanine instead off an on-the-shelf ADC mezzanine :

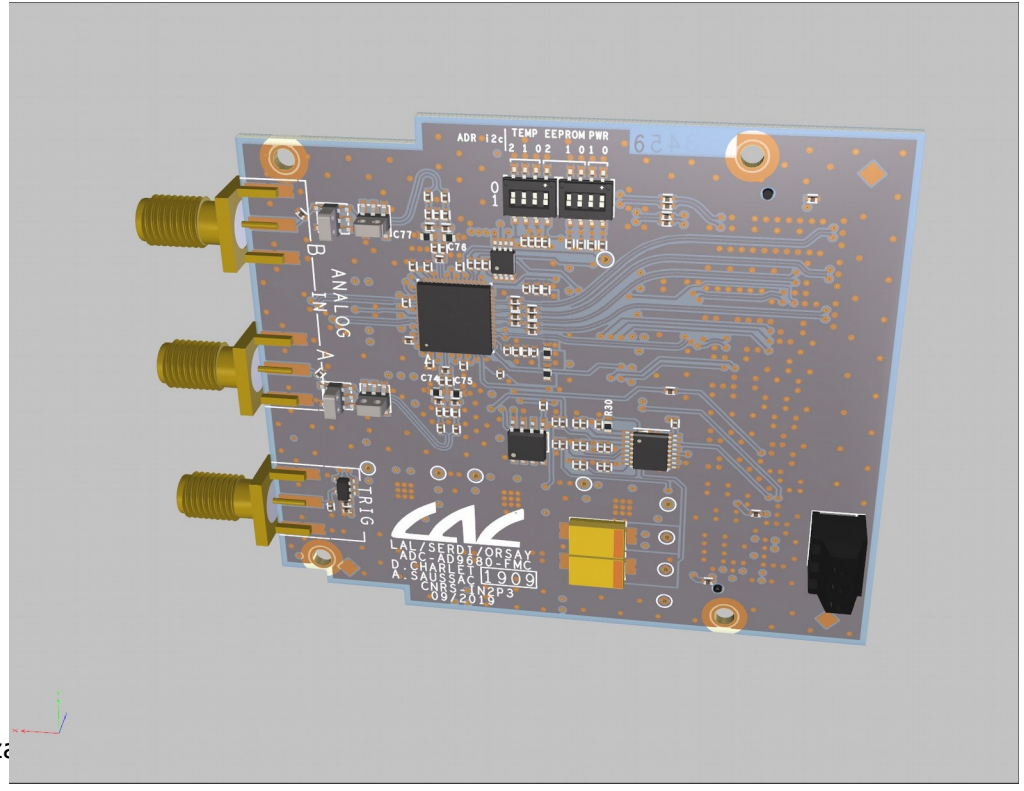
- include own PLL.
- ADC clock source : External clock

- Mezzanine main features :
  - VITA57.1 (FMC)
  - ADC 9680
  - 2 channels
  - 14 bits
  - 1.25 GSPS
  - JESD204B
  - 2GHz analog bandwidth
  - External trigger in

Status Mezzanine ADC



- PCB : 4 Layers
- Schedule :
  - Production of 2 prototypes : October.
  - Test : mid November.
  - Production of 6 boards : Beginning of 2020.



Conclusion

- IDROGEN-2 is being produced
- WhiteRabbit firmware adapted on ARRIA10
- Most firmware blocks written and tested, but full integration is to be done.
- IDROGEN-2 available beginning of 2020.
- ADC board available beginning of 2020

- OXIGEN (Xilinx-flavor IDROGEN) development will start soon.