H21/CRT electronic development status in France

CRT meeting - 13 November 2008

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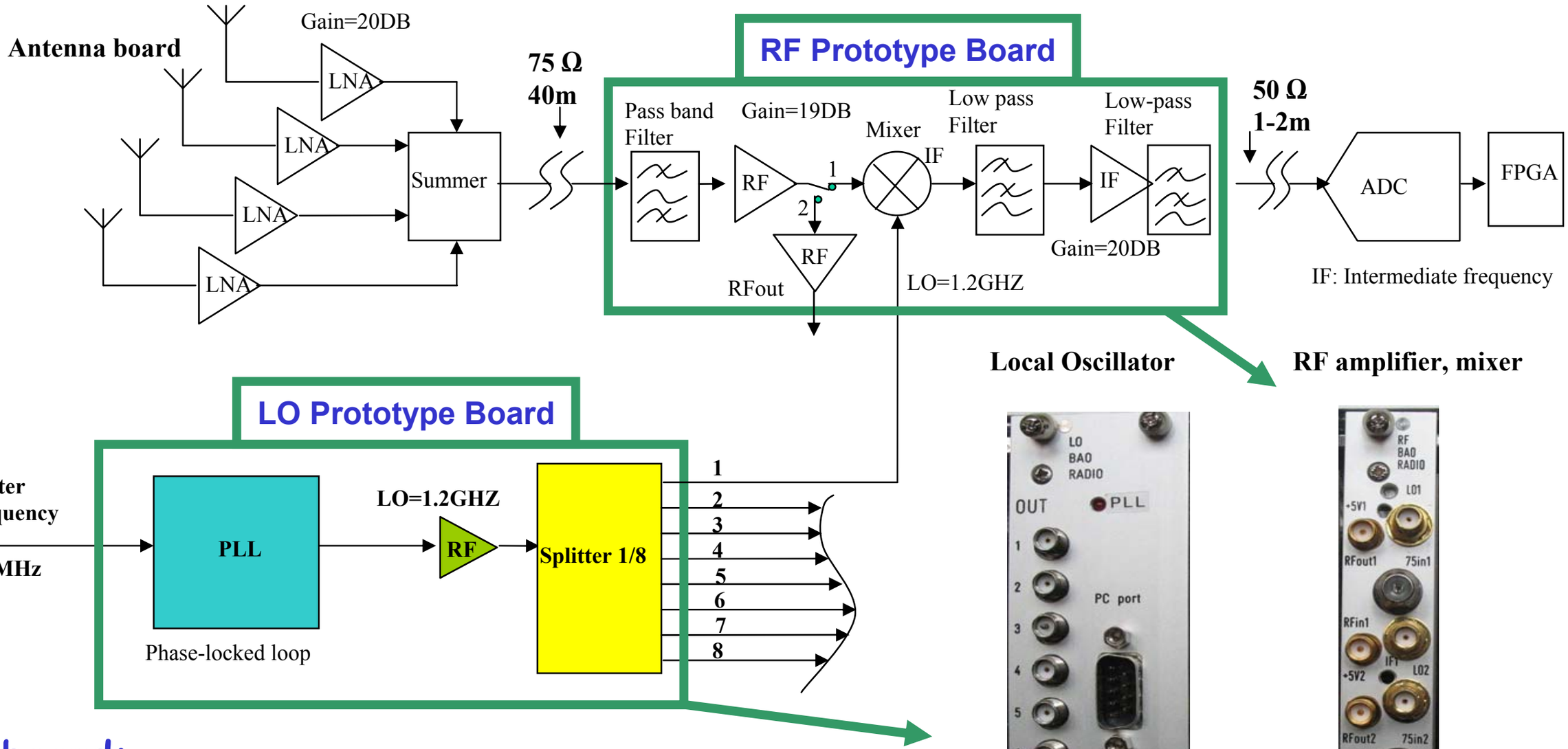
Electronic chain modules

- AEM : Analog Electronic Module (Amplification, filtering, frequency shifter)
- DCLK : Clock and trigger distribution system
- DFS : Digitizer Frequency Separator (ADC-Board) 4 channel, 500 MHz sampling, with on the fly FFT capability, dual high speed optical data transfer
- PDR : PCI-Express data reception module

Analog chain for the RF prototype Board

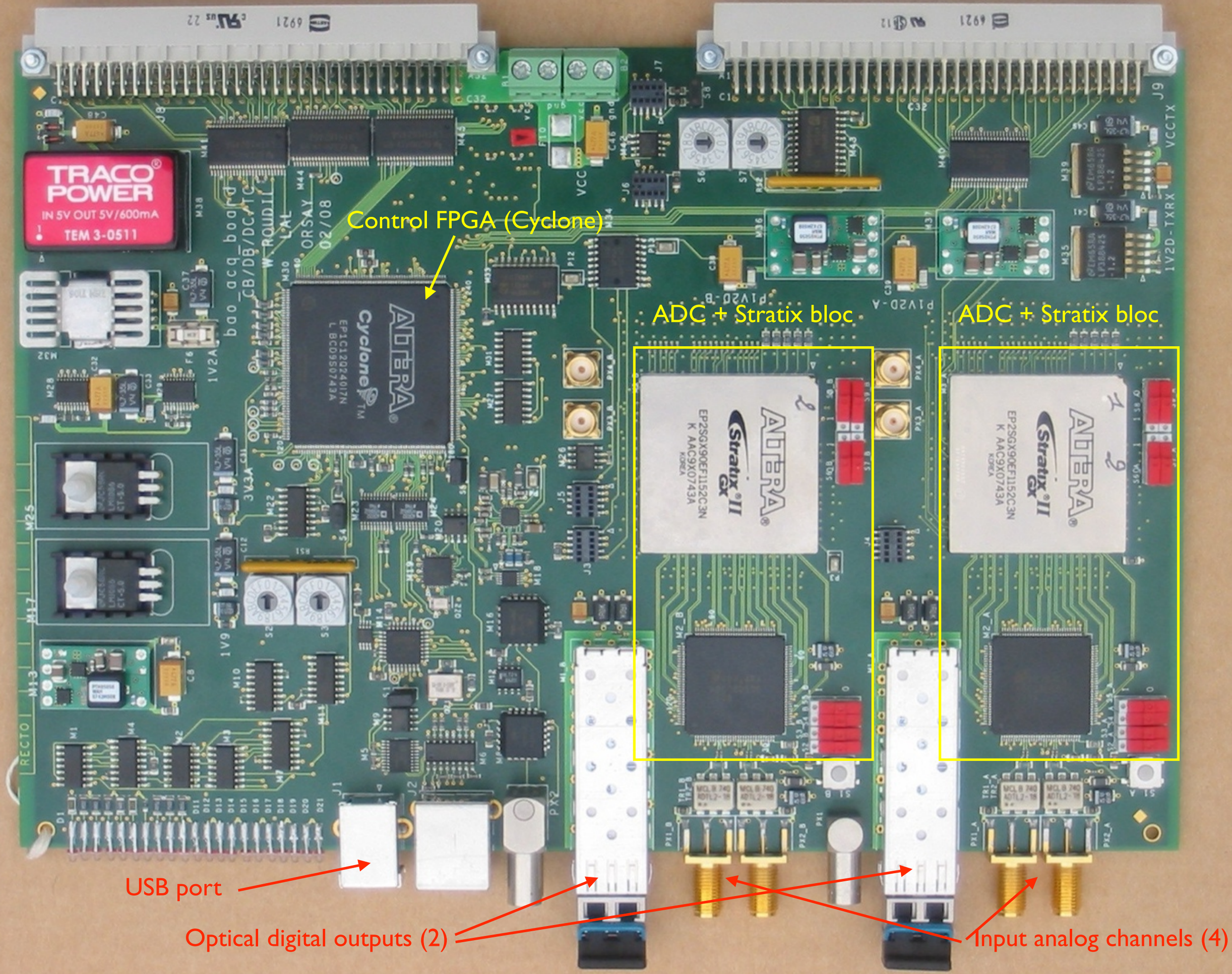


Front panel plug-in (3U EuroCard)

RF board:

- 75Ω/50Ω inputs
- 2 channels per board
- Possibility of by-passing mixer to test the under-sampling approach.
- Possibility to "tune" the pass band filter

DCLK


Control FPGA (Cyclone)
ADC + Stratix bloc
ADC + Stratix bloc
USB port
Optical digital outputs (2)
Input analog channels (4)

AEM (Analog Electronic)

- Filters have been redesigned to increase out of band rejection (in particular the LO - Local Oscillator rejection)
- Use of higher quality components (L,C)
- Test/validation of the possibility to use undersampling (without LO)

Clock Distribution

- Test of DISTCLK system with DFS (ADC-board)
- Current operating mode (next few months) : 50 MHZ clock provided to the DFS , as well the Trigger=StartAcq (TRG) signal. Each digitization frame (packet) is started by the TRG signal

DFS (ADC-Board) - I

- Test and correction of on board PLL parameters (500 MHz ADC-clock , 125 MHz FPGA clock and 125 MHz serial link clock are generated on board
- Input stage (analog) redesigned to push the input bandwidth above the current 1 GHz limit
- Small corrections/repairs : all 4 channels on each of the two prototype boards are now working

DFS (ADC-Board) - 2

- Implementation of on the fly FFT on the FPGA.
- The firmware performing 4096 points FFT on the 2 ADC channels, on a single FPGA, in streaming mode is now working.
- FFT-firmeware is being evaluated and debugged through the USB interface

PDR (PCI-Express) **firmeware**

- A new firmeware architecture has been designed and implemented to reach maximum bus capability
- The new architecture uses SGDMA (Scatter/ Gather DMA), and can in principle handle up to 64 kB/128 kB data packets
- Sustained data transfer rate of ≥ 600 MB/sec has been demonstrated during tests on Dell PowerEdge 2900

On going work ...

- Tests with two PCI-Express boards on a single Dell PE2900 shows excellent performance → 500 MB/s per board
- Redesigned, more flexible acquisition/processing software (C++ , multithread)
- Tests under way to check data synchronisation with multi-channel acquisition in the lab
- Test at Nançay scheduled first week of December
- If OK, plan test campaign at Pittsburgh with 8 channels + beam-forming on PC's, as soon as possible, beginning of 2009

Short term plans …

- We are building a 32 (+8+8) channel system :
  - 8+2 = 10 additional PCI-Express board ordered (
  - Critical components (ADC's, FPGA) ordered for 8+2 = 10 additional DFS (ADC-boards)
  - All corrections / modifications included in the PCB design.
  - Fabrication of 2+8 = 10 DFS boards will be initiated soon
- Design and firmeware test work on FPGA based correlator / beam former
- As a consortium or collaboration :
  - Try to define a common/reference system architecture and components