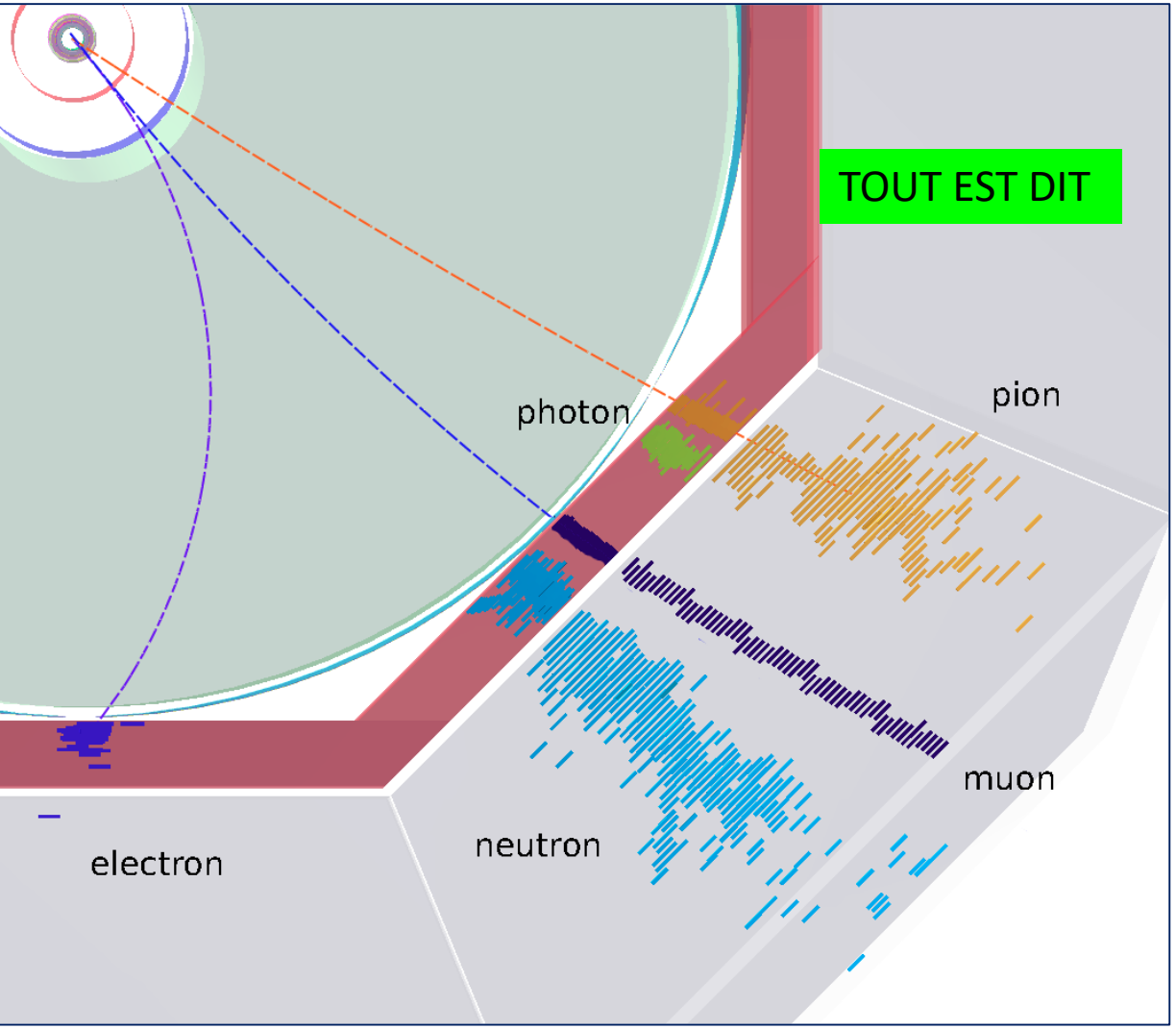
SiW ECAL R&D

Particle Flow Algorithm*

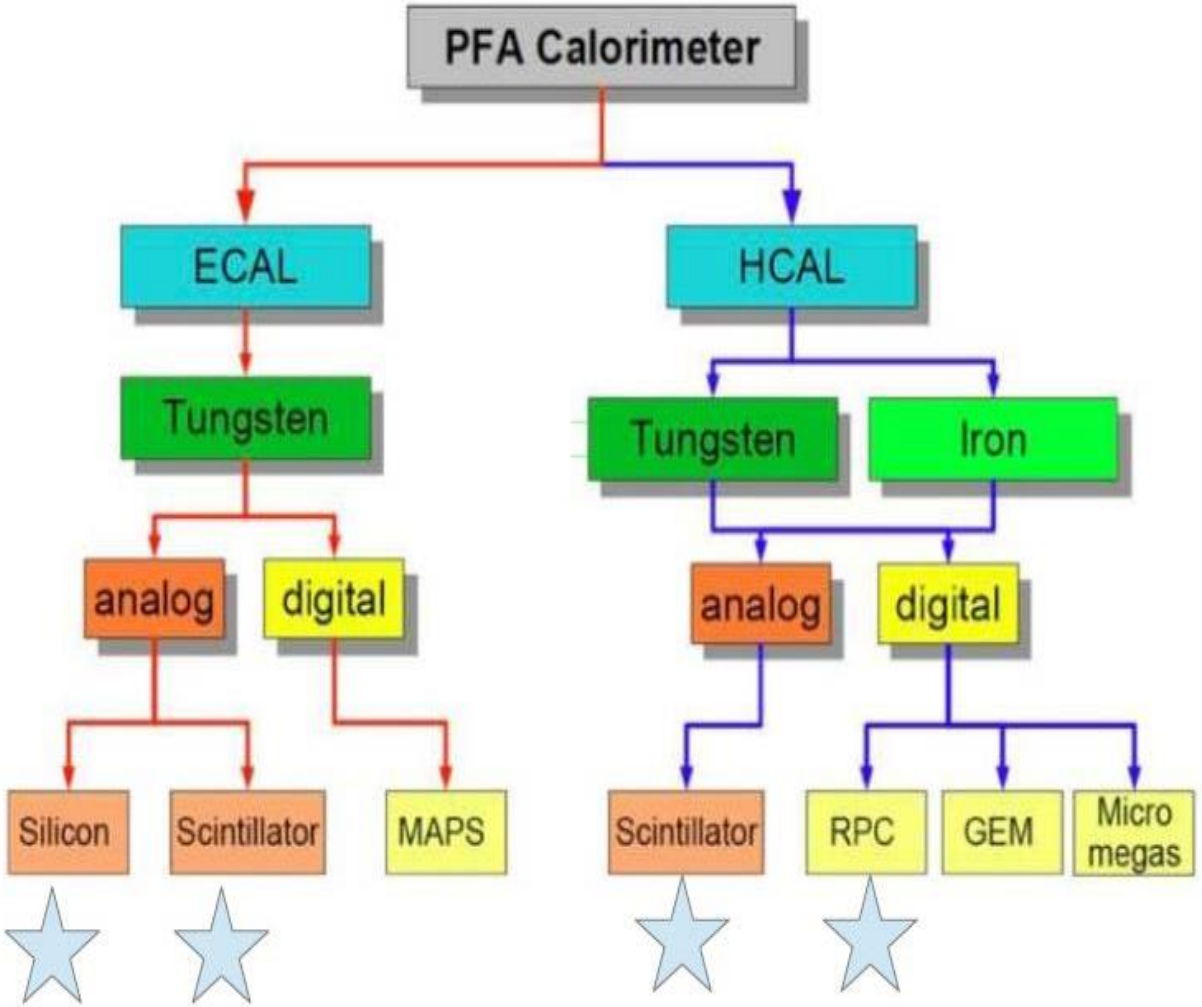


A l'ordre 1,
L'important est de connaitre
les particules "stables" dans l'état final
Avec une estimation correcte de
la direction / énergie

Au second ordre,
Avoir la meilleure qualité possible
de la mesure l'énergie (4-vecteurs)

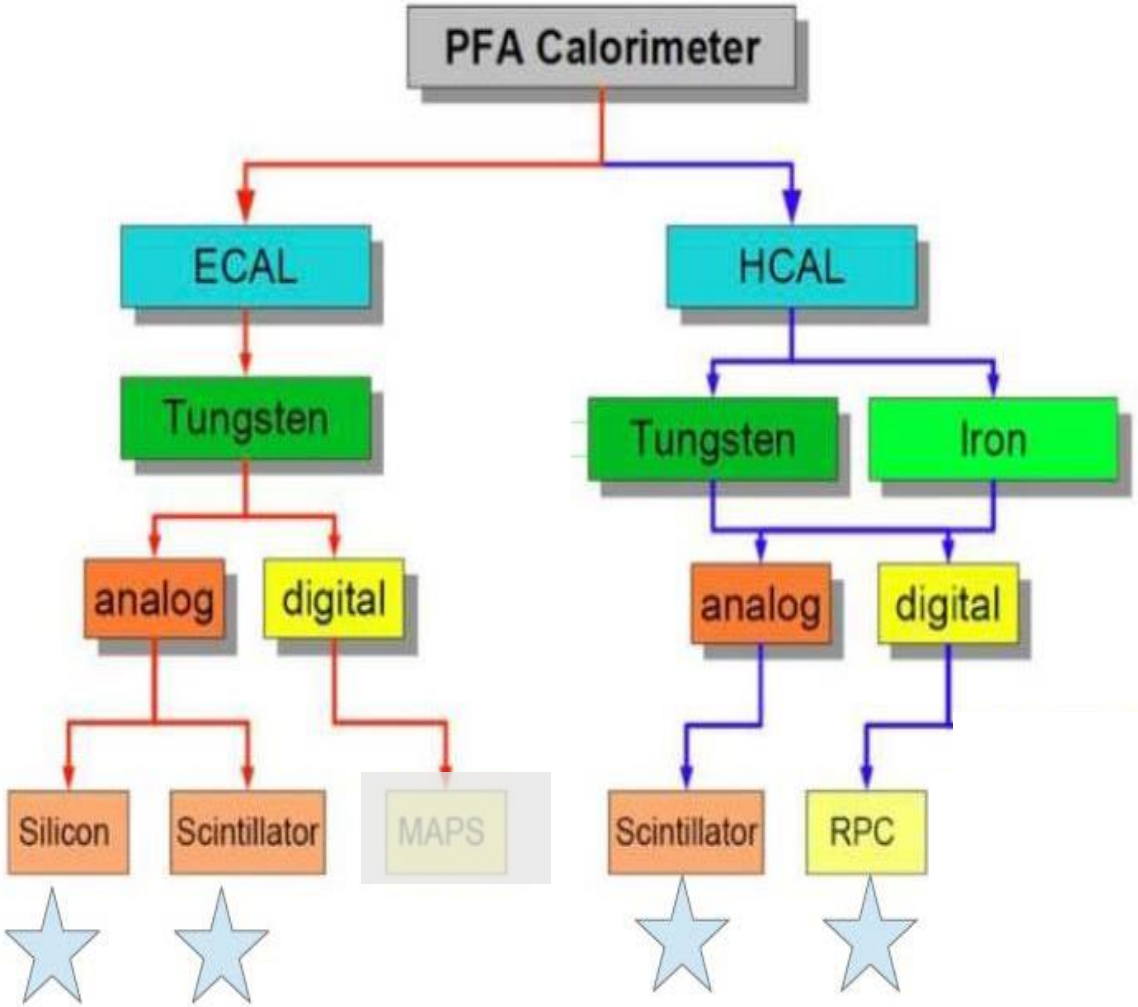
Certaines études sur FCCee prônent
du cristal pour avoir le meilleure second ordre
Mais oublie l'ordre 1 !! C'est une erreur
Ne pas oublier les leçons du LEP (ALPEH vs L3)

- Développé par le LLR dans ALEPH pour la physique des taus et des jets en 1990
  (Thèse de F.Braems « Recherche de nouveaux leptons avec le detecteur aleph au lep »)
- Adapté/étendu au projet TESLA en 1999 – DESY report 2000



More than 300 physicists/engineers from ~60 institutes and 19 countries coming from the 4 regions (Africa, America, Asia and Europe)

All projects of current and future high energy colliders propose highly granular calorimeters



More than 300 physicists/engineers from ~60 institutes and 19 countries coming from the 4 regions (Africa, America, Asia and Europe)

All projects of current and future high energy colliders propose highly granular calorimeters

Contexte scientifique

Basé sur le concept le PFA, concept maintenant utilisé comme Baseline sur tous les projets de collider

Calorimètre plus proche d'un appareil photo que d'un thermomètre.
Avec le timing du signal, on sera plus proche d'une caméra

Pour faire quoi ?
Séparer les particules, les identifier et avoir une mesure correcte de leurs énergies

Pour quel physique
Nombreux domaines collider pp ou e+e-
neutrino physique sur accélérateur (detecteur proche)

HL-LHC , upgrade de CMS end-cap
FCCee, CEPC, ILC ou CLIC

Calendrier

- Possiblement court/moyen terme avec des discussions sur le near detector de DUNE, LUXE (DESY), etc …

- Incertain pour le futur collider, MAIS
  Il est nécessaire d'avoir des certitudes de faisabilité et d'adaptation aux expériences

Exemple : ILC …. Powerpulsing et timing possible
CEPC/FCCee ….. Active cooling « a la CMS », timing mandatory, large data flow (Z peak)

Notre calendrier

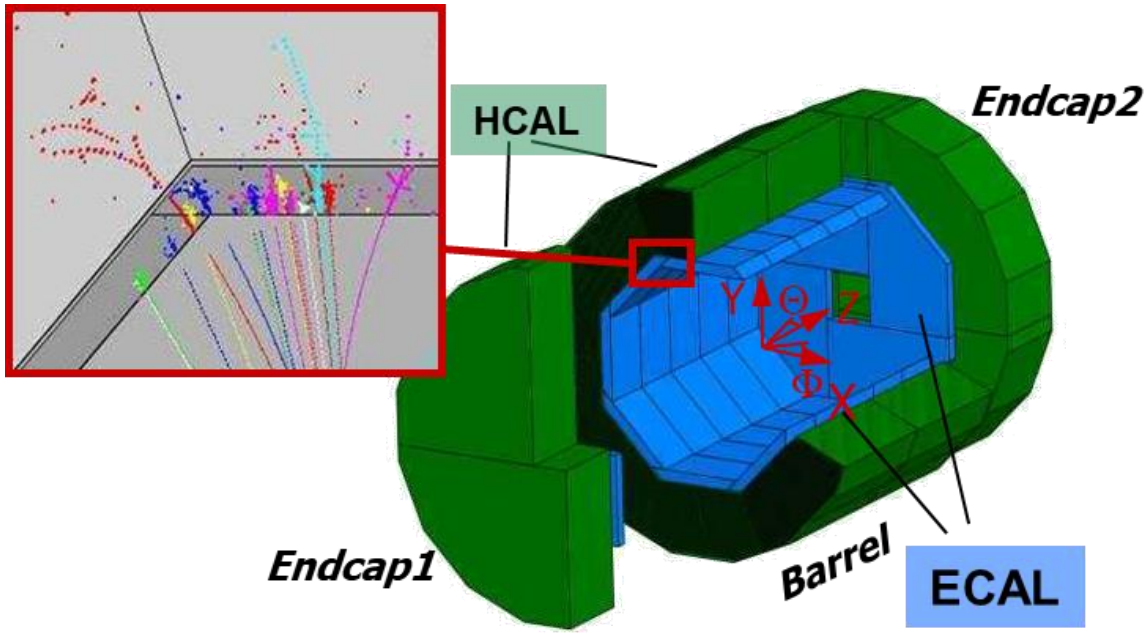
- Test beam proto actuel **2022**
- Prototype aussi proche que possible d'un détecteur « scalable » **2023**
- Test beam module 0 **2024-2025**

en rapport avec les proposal ILC, CDR de FCCee

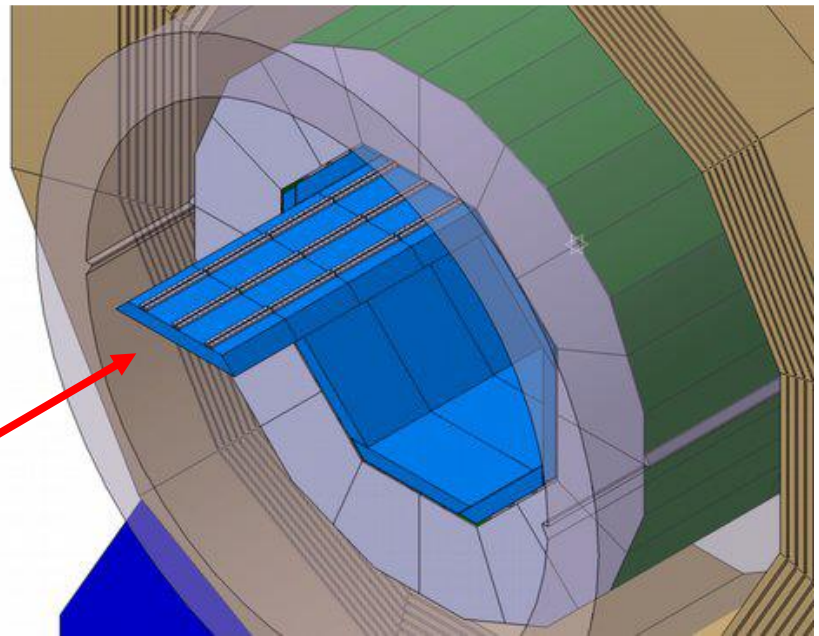
Quel ECAL

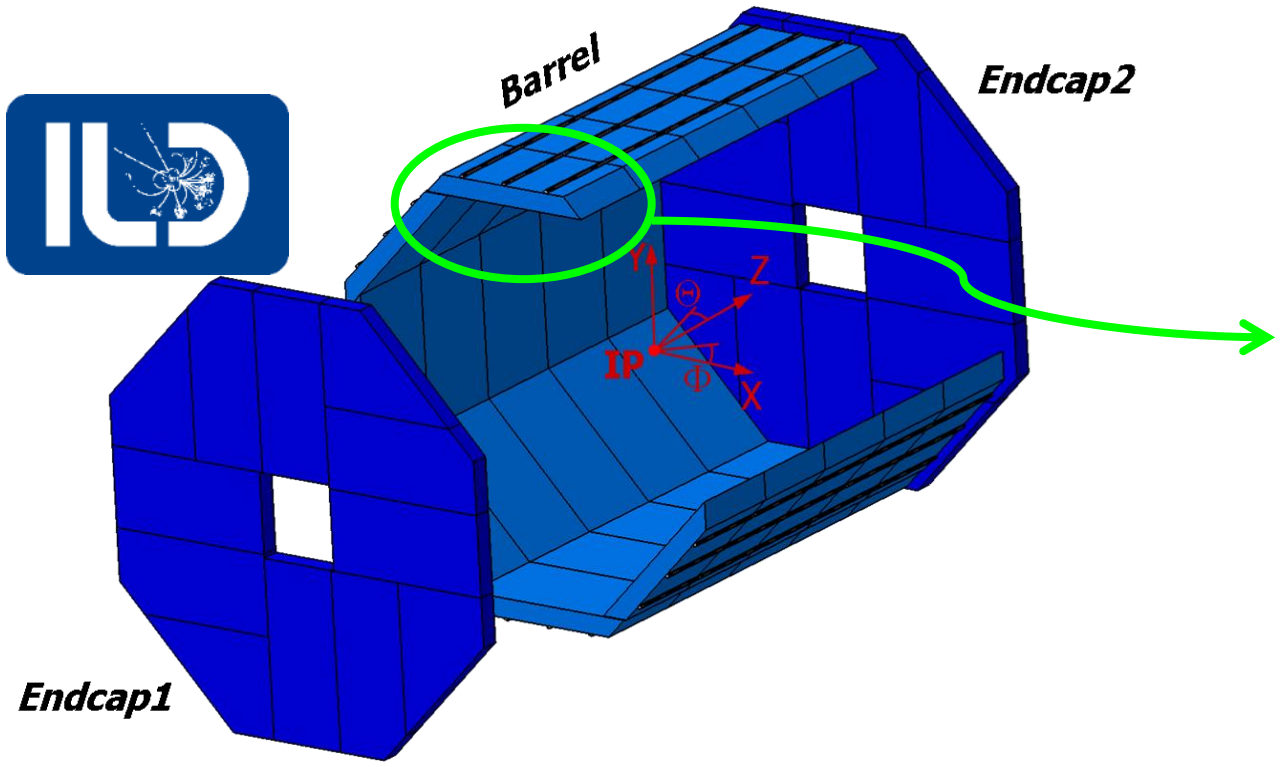
En chiffres , sur le calorimètre final

- 20 a 30 couches de lecture dans 20 à 25 cm d'épaisseur
- 50 a 100 millions de canaux de lecture
- 100 tonnes de tungstène
- 1200 à 2100 m² de silicium détecteur (selon rayon et longueur)

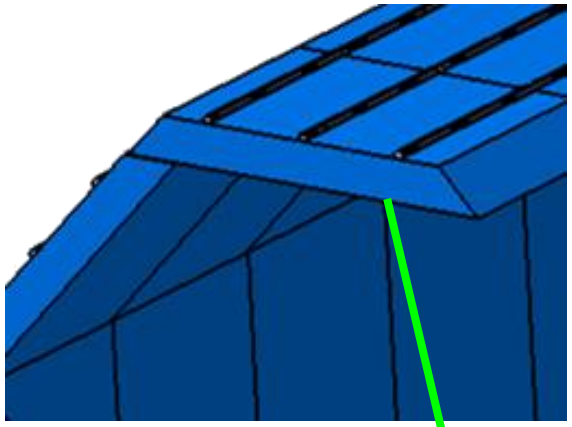


MODULE ECAL

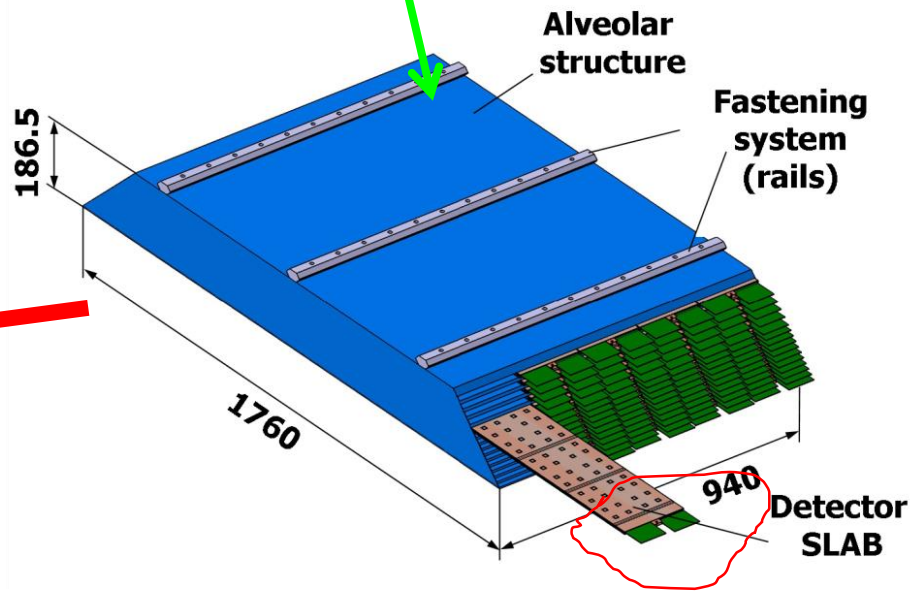




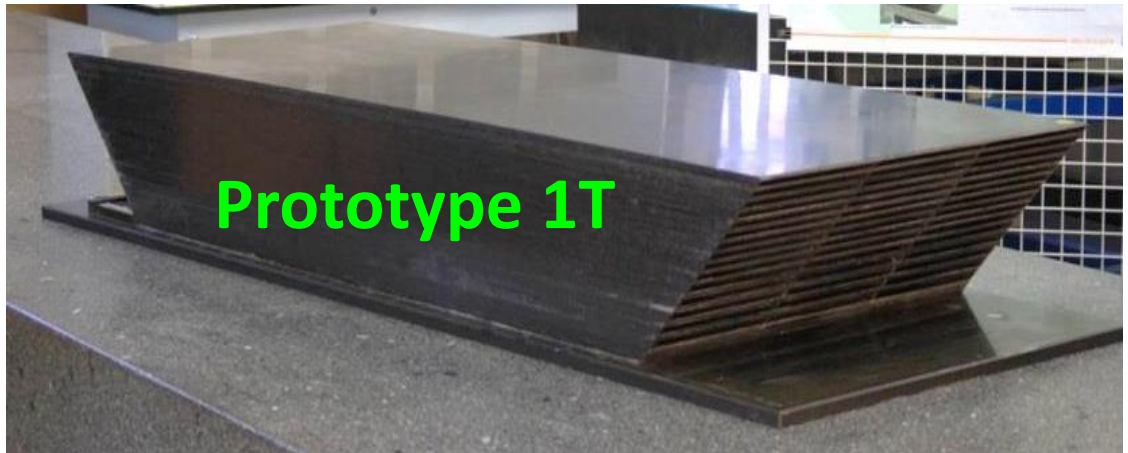
No DEAD ZONE !!!



MODULE ECAL

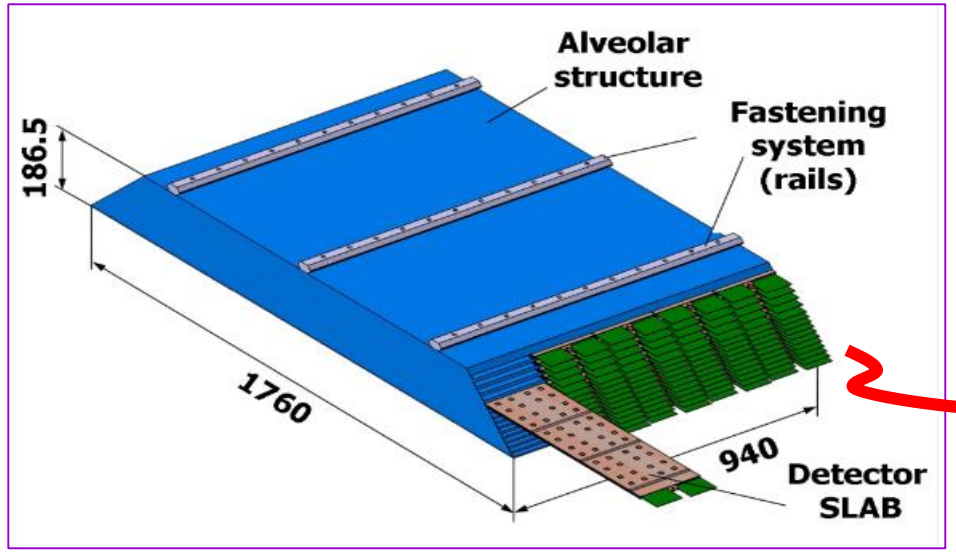


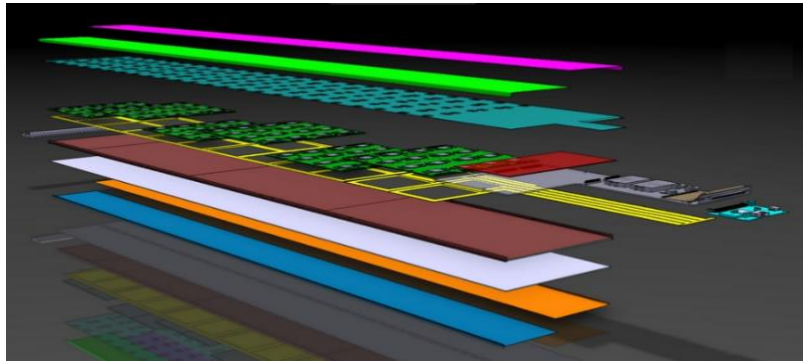
Carbon fiber –Tungsten structure with Alveola to slide in the active layers.

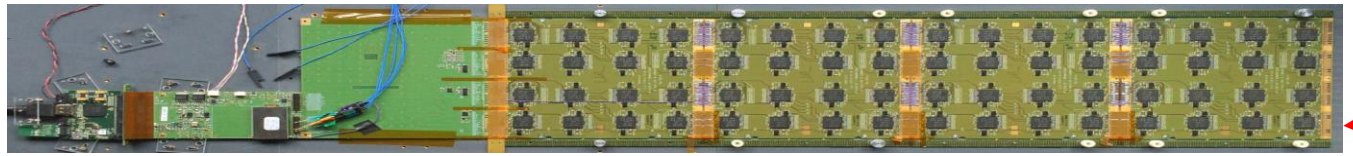


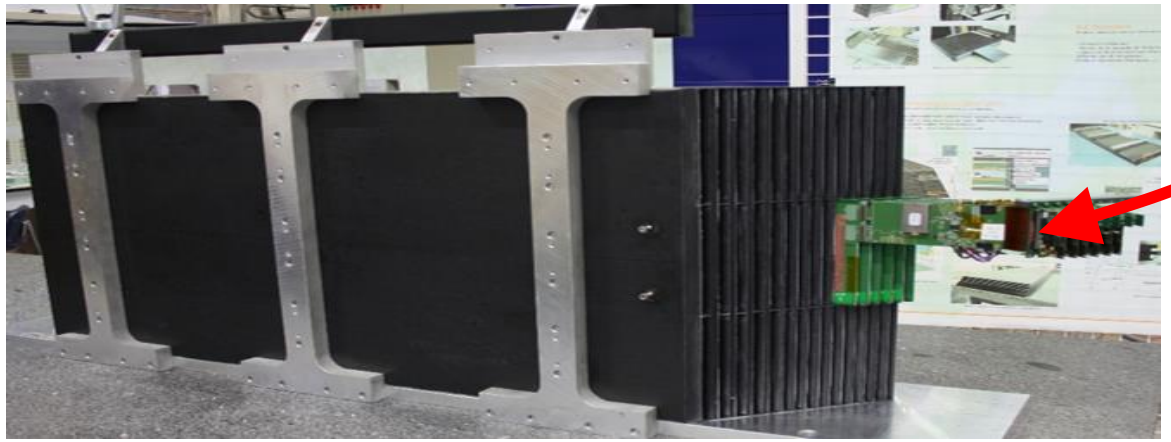
MODULE ECAL

Electronique readout DANS le détecteur

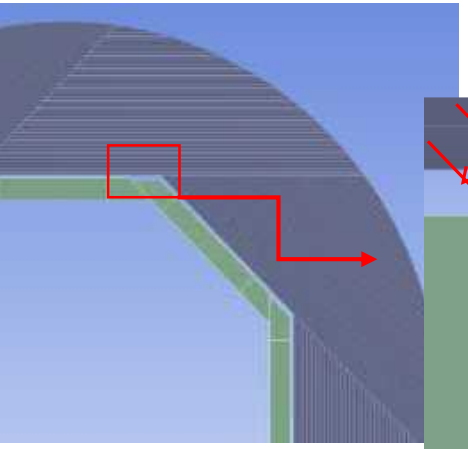


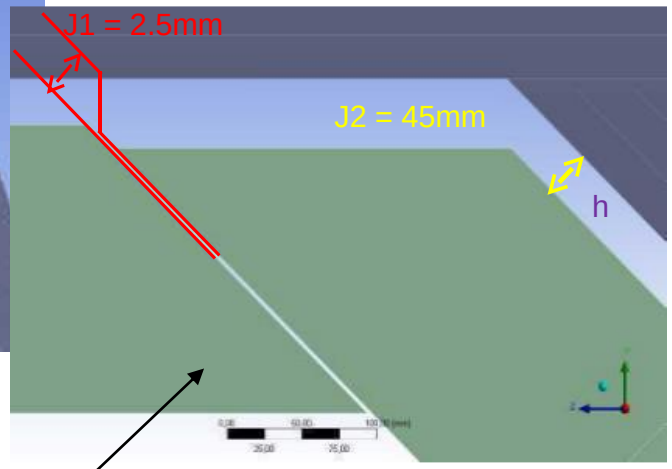


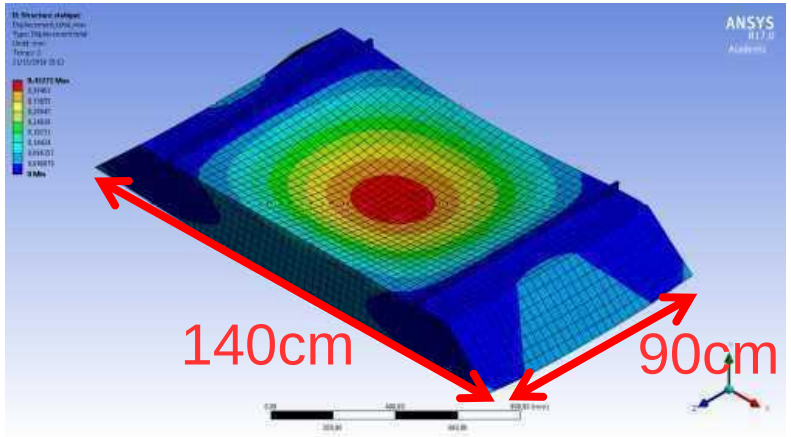


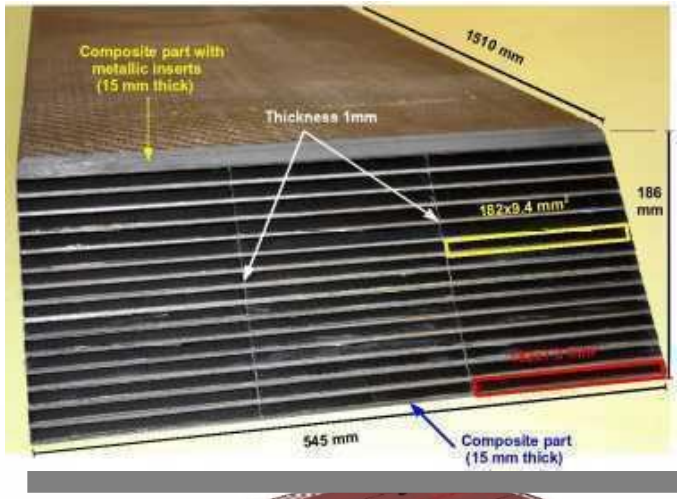


@LPSC







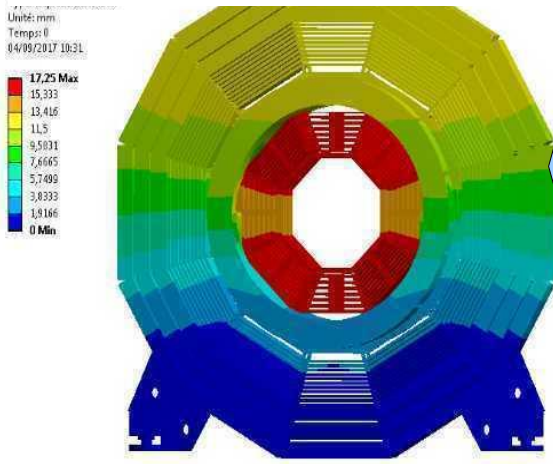


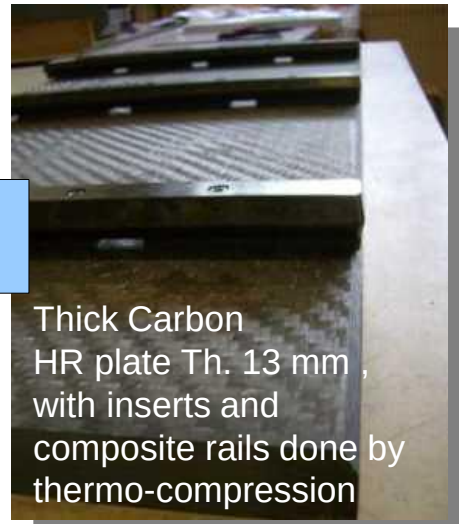
J1 = clearance between modules for the ECAL

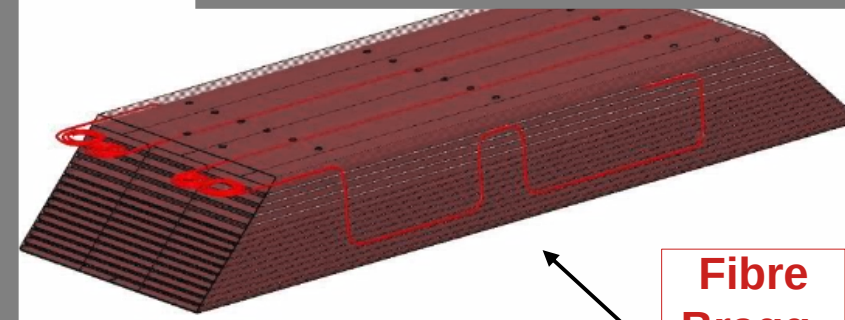
J2 = Clearance at ECAL edges between ECAL and H

h = height of the rails 30mm

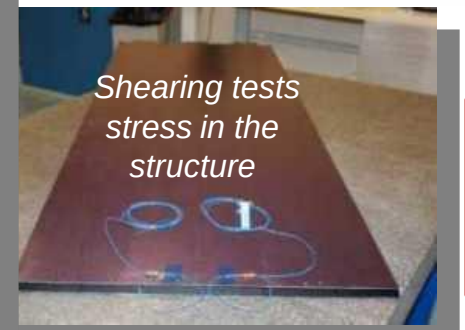
Static & Dyn. Simulations







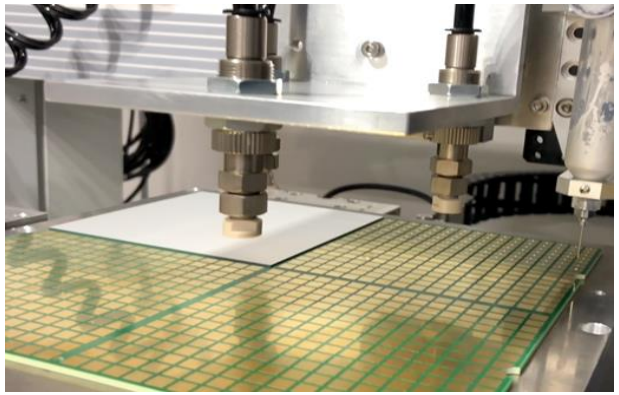
Fibre Bragg-Grated



measurements still to be done...

Développements technologiques

- Silicon wafers ≥ 1000 m² et utilisation de wafers de 8'' (très différent des 6'' selon CMS)
  (effet de bord du champ E (reliée a la taille des matrices) , solidité , flatness,…)
collage sur PCB avec colle conductrice (EPOTECH) – ROBOT **(LPNHE)**



- ROC - readout chip multi canaux analog + digital !!! (remerciements de CMS à CALICE)

Nouveautés : coherent noise , S/N @mip and 25nW/canal (avec PP) avec le internal self triggered decision
CMSHGROC … **OMEGA (Ω)**

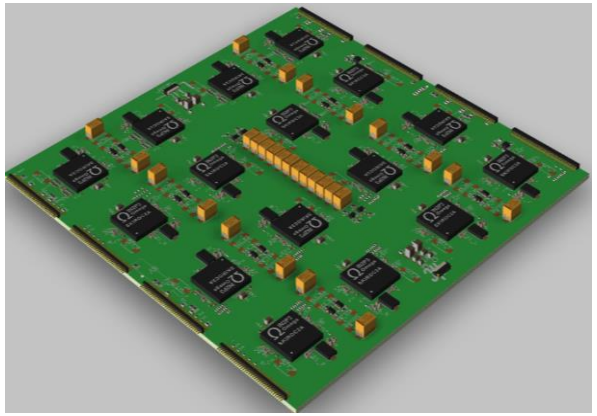
- PCB ultrafin (et COB) **(LLR , IJCLAB, Ω)**
- Long slab (chainage de PCB sur 2m) **(LLR, IJCLAB, Ω)** et etude du refroidissement **(LPSC)**
- Self sustainable mechanics based on CFi and tungsten plates
  (NO DEAD ZONE !!!) **(LLR, LPSC)**
- SL DAQ board 4x18 cm² (**IJCLAB)**

Développements technologiques

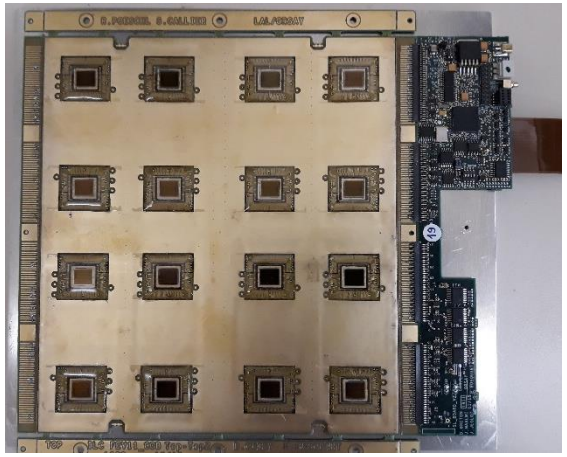
front-end board (FEV2.0) 1.6 mm

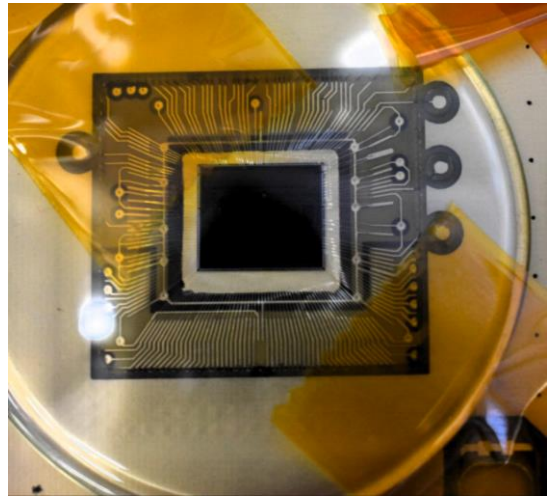
- Dedicated and designed for long SLAB (up to 10 boards chained)
- New LV power distribution for power-pulsing
  - 1 analog “regulateur de tension” (LDO) per chip
  - 1 digital LDO per 4 chips
  - Optimize capacitance value as battery
- Add buffer for slowcontrol
- Modify HV distribution for wafer
  - FEV drive HV instead of kapton
  - Add HV filter per wafer
- SK2A chip with thinner BGA packaging (1mm)

New SK2A package



front-end board COB 1.2 mm





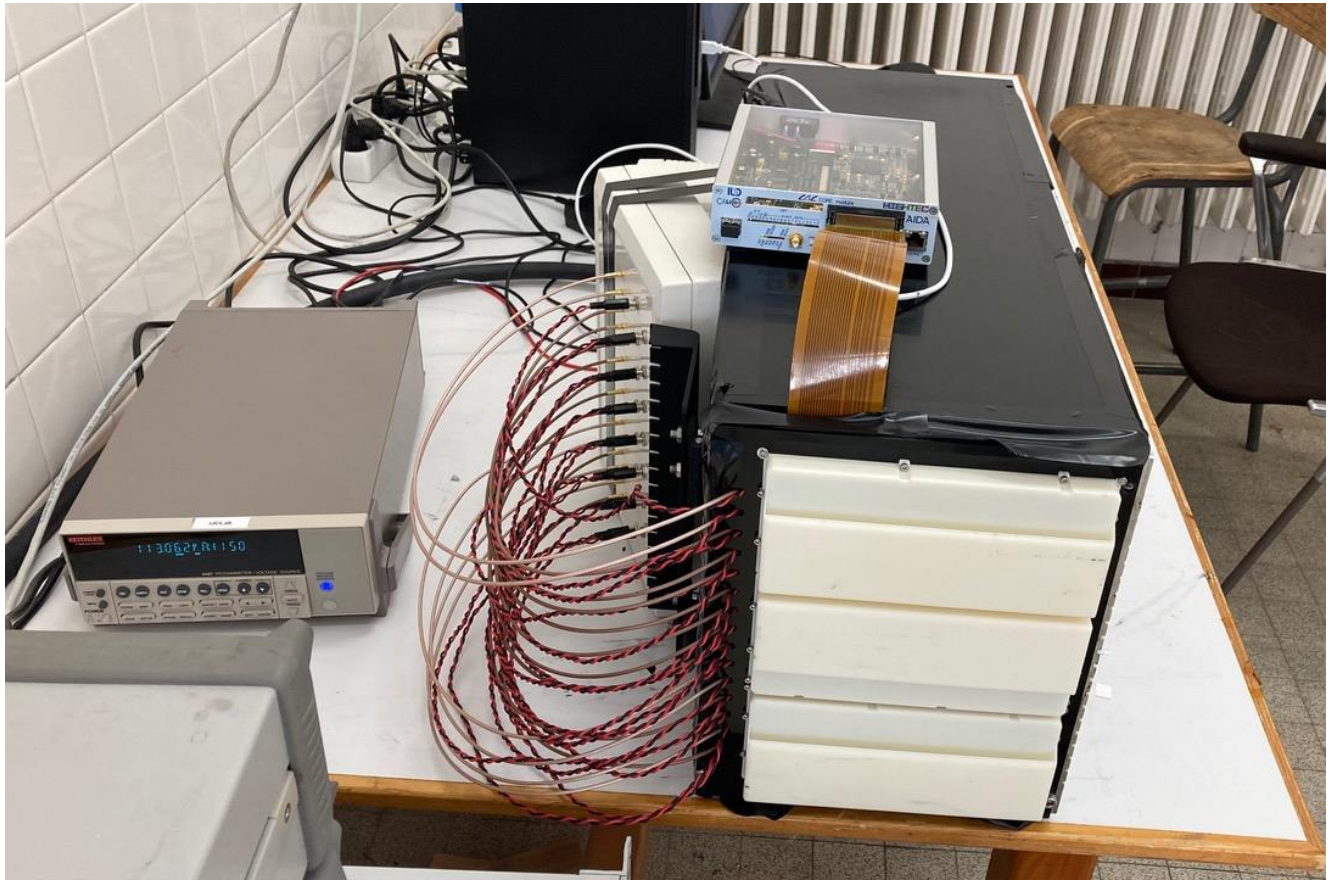
- ASICs wirebonded in cavities
  - COB = Chip-On-Board
- External connectivity compatible with BGA based FEV10-12
- Encapsulation a IJCLAB

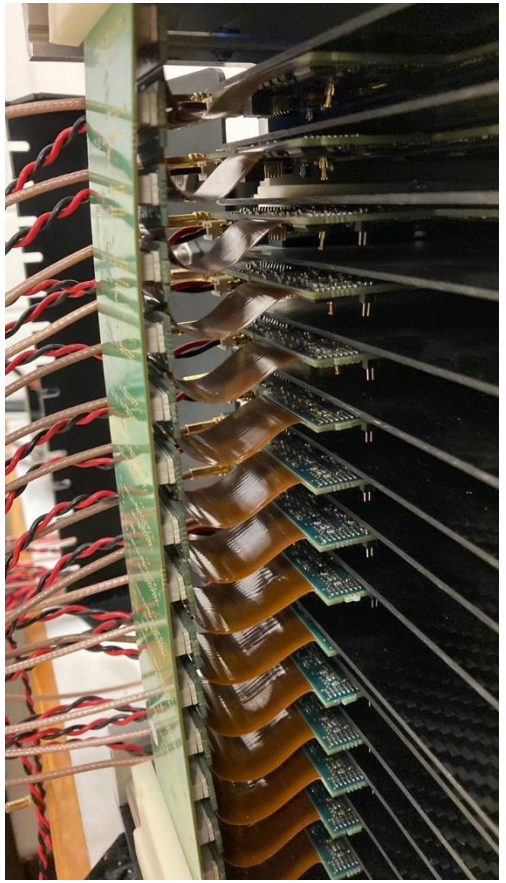
A complete study of mechanical and Industrial aspect to be done

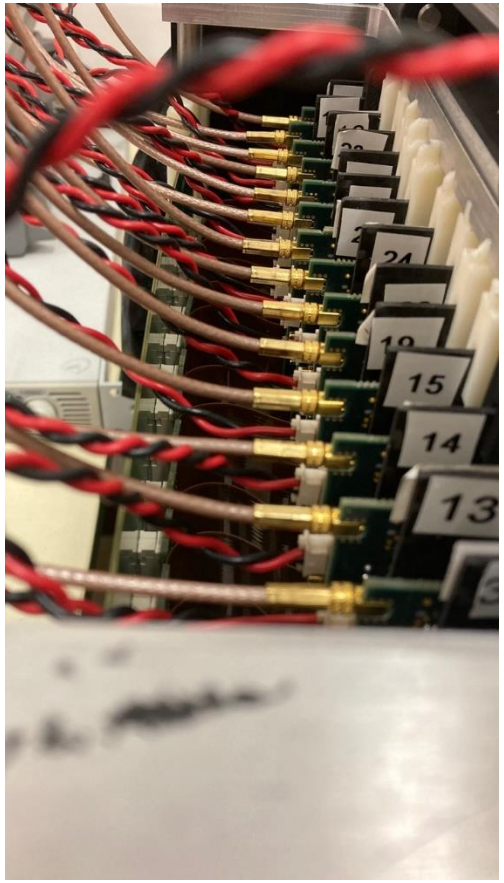
Le prototype 15 couches

- Mounting of stack summer 2021
  ... including two slabs repaired at LPNHE over Winter/Spring 2020/21

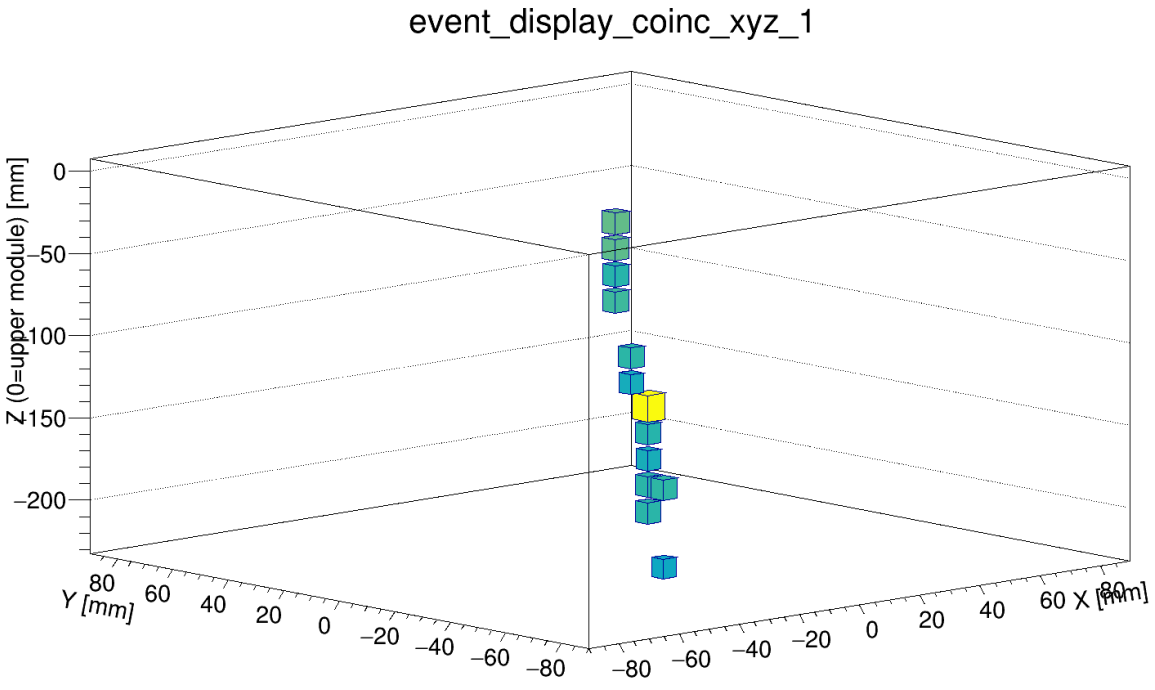
- **15 layers** which correspond to **15360 cells** (readout : pas de cable, juste kapton et fibre optique)

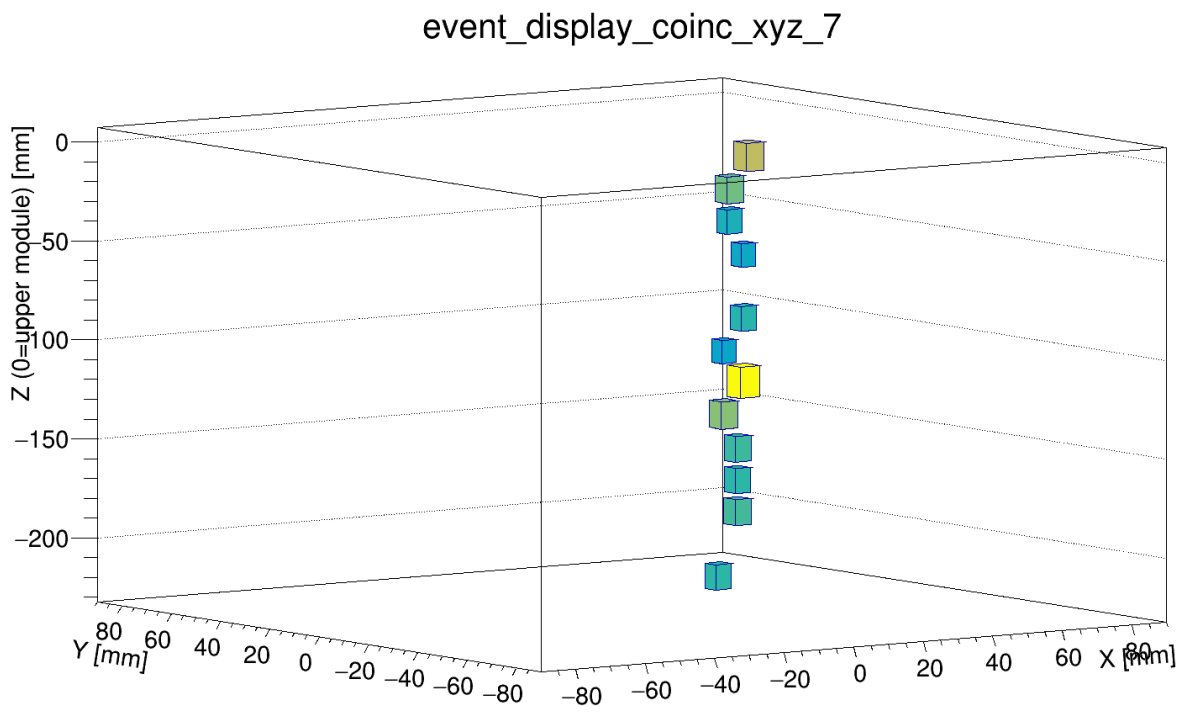






- Since 18/6/21: Data taking with cosmics and systematic characterization





C’est du muon cosmic, donc du MIP

Ce que dit l’event display,

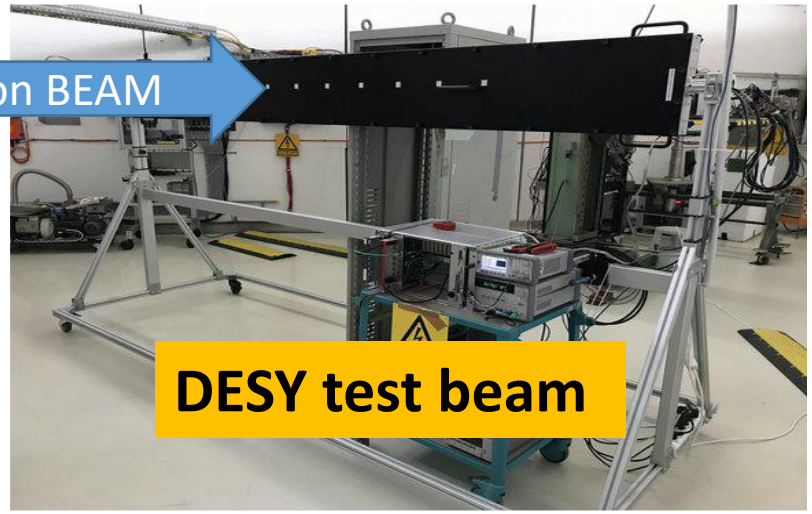
On peut avoir une bonne efficacité au mip et pas/peu de bruit

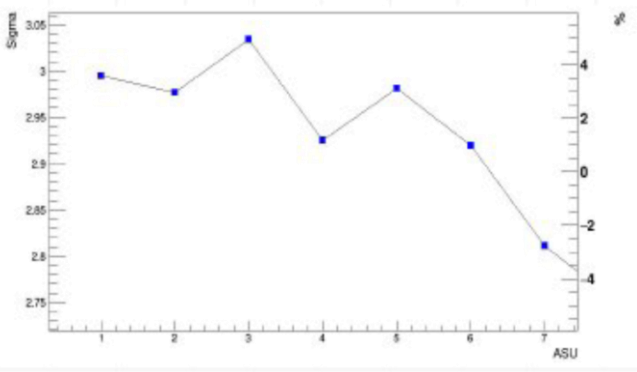
FUTURE proche : (si COVID …)

Full scrutinisation in upcoming beam test at DESY and in further beam tests in 2022 at DESY and at CERN

long slab

- Electrical prototype v1.0:
  - Chained 8 boards
    with 1 small Si matrix/board
  - Measure MIP on each wafer
  - Measure voltage drop





- **New LONG slab v2.0:**
  - Design fake FEV2.0 with connector for mechanics/ HV test
  - Start LONG Slab electrical prototype assembly
    - Measure DC voltage
    - Measure new LV distribution
    - Test configuration on 10 boards chained
    - Measure HV propagation
    - Test readout of 160 chips chained
  - Start physics with unglued wafers

Maturité technologique

Millions de canaux sur un calorimètre implique de la R&D

- Le contrôle du bruit cohérent
- Engineering (extraction de millions de canaux, powerline, …)
- S/N au mip
- Capacité de sparsification (local zero suppress high eff. , low noise)
- Capacité de DAQ sur des millions de canaux
- calibration, stabilité, linéarité
- capacité industrielle et contrôle qualité (prix du silicium, des chips, etc…)

Maturité technologique

En partie “traité” par CMS-HGCAL

Millions de canaux sur un calorimètre implique de la R&D

- Le contrôle du bruit cohérent
- Engineering (extraction de millions de canaux, power lines, …)
- S/N au mip
- Capacité de sparsification (local zero suppress, high eff. , low noise)
- Capacité de DAQ sur des millions de canaux
- calibration, stabilité, linéarité
- capacité industrielle et contrôle qualité (prix du silicium, des chips, etc…)

conclusions

Depuis CALOR 2000, L'IN2P3 était la référence sur le PFA et l'ultragranulaire

Est-ce encore le cas ?? « La nature a horreur du vide »

Futur proche

- Malgré l'absence de soutien RH depuis 10 ans, on a fini par arriver (lentement) à un proto de 15 couches , avec electronique intégrée, powerpulsing, un S/N > 10@mip …. **TEST BEAM** … conclusions sur le système, l'épaisseur, la mécanique des « slabs », …

- **En parallèle,** nécessité de développement de soft et algorithmes pour complétement analyser les TB

Futur moyen terme:

- BESOIN d'un chip VFE ROC nouvelle génération incluant une chaine TDC (SK2A est en SiGe 350nm … le timing n'a pas fait partie des priorités)

- La mécanique W-CFi et le cooling est à l'arret depuis 5 ans environ !! (pourtant pour le FCCee…)

- Développement temporelle des gerbes !!! Versus G4 et versus une utilisation potentielle dans le PFA, PID !!

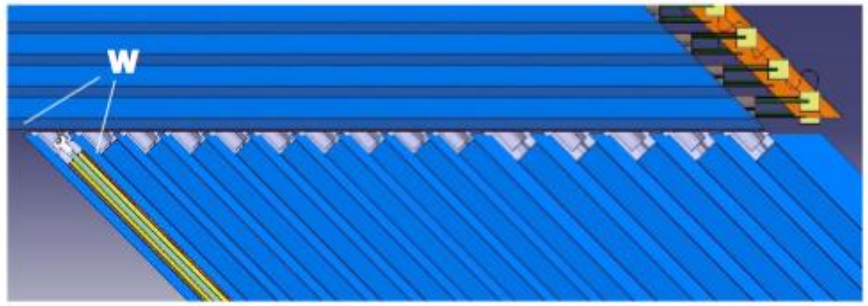
Could it be for FCCee ?

or CEPC !!

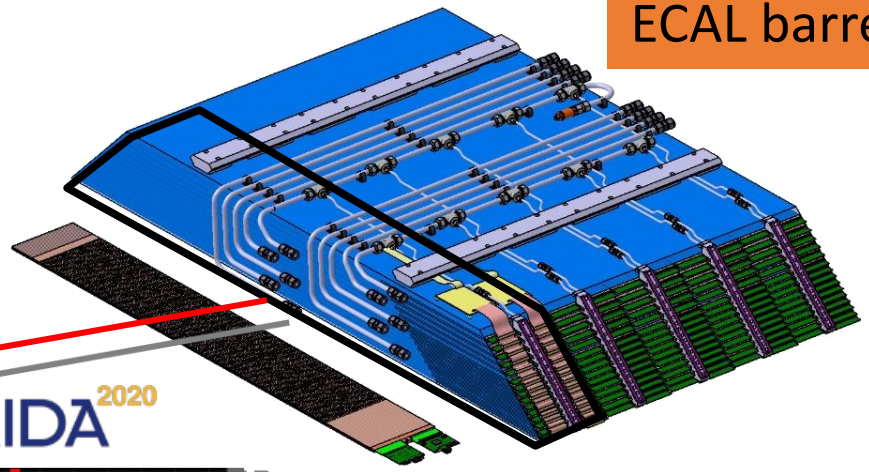
MODULE ECAL

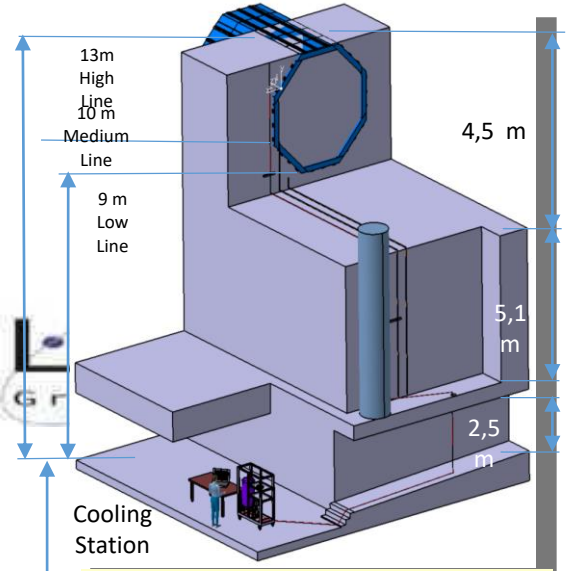
Avec cooling passif

Design/etude LPSC

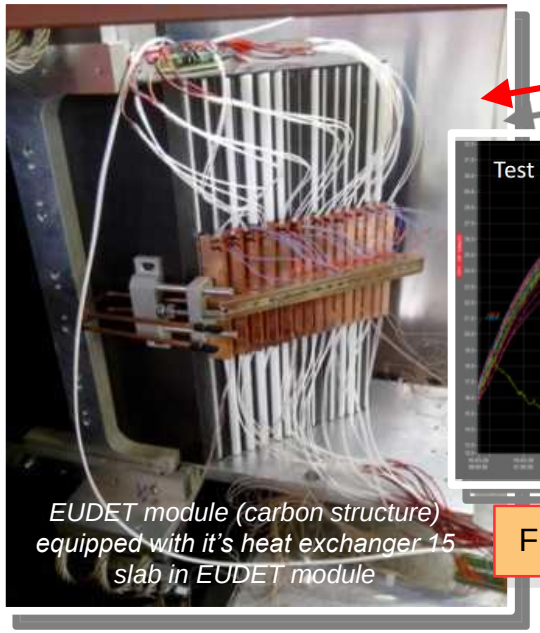


ECAL barrel



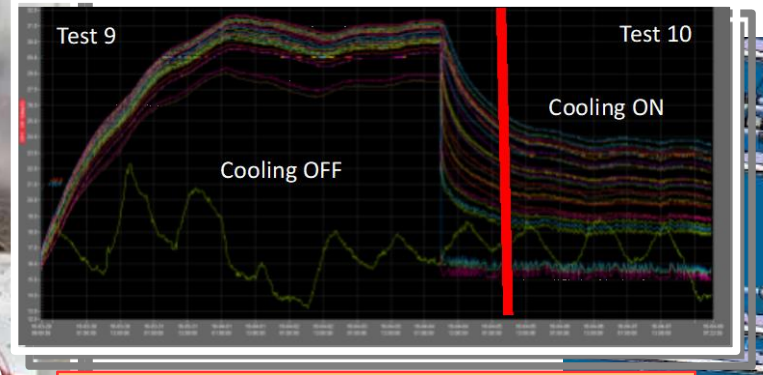


LPSC cooling test area with a drop of 13 m



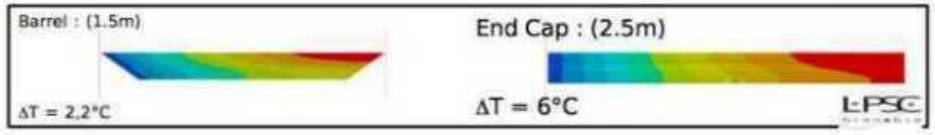
EUDET module (carbon structure) equipped with it's heat exchanger 15 slab in EUDET module

AIDA 2020



First tests results in line with simulations

ECAL end cap

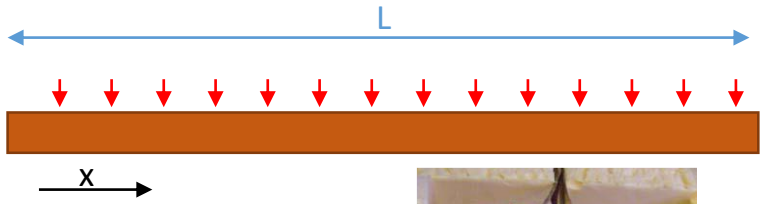


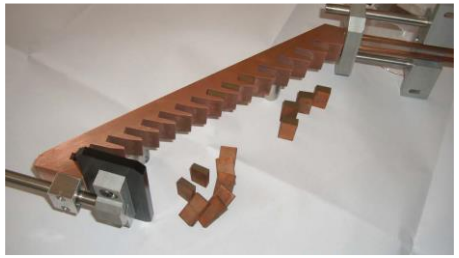
http://cds.cern.ch/record/2624680

ECAL cooling studies

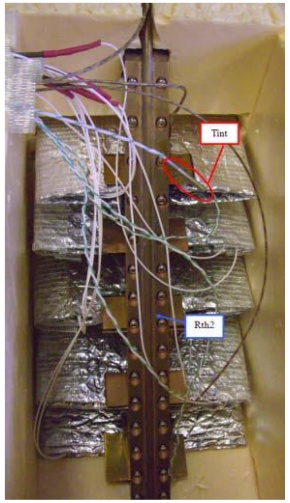
Passive cooling

(ILC)





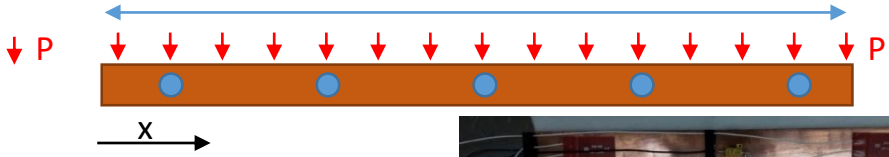
Passive cooling ramp example



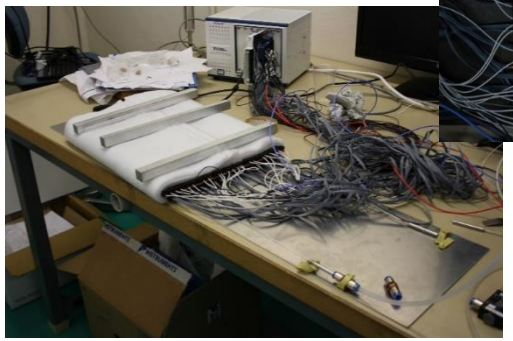
Passive cooling ramp set up test

Active Cooling

(CEPC, FCCee or CLIC)



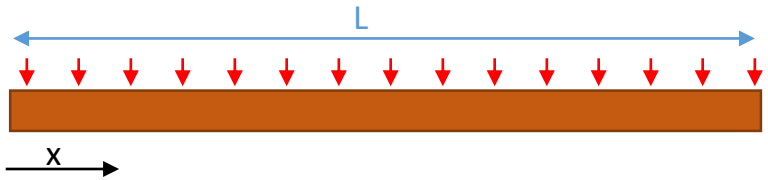
Active cooling test layout (400mm x 300mm x 3mm thick copper plate with 1,8OD pipes embedded)



Active cooling set up test with water at room temperature

Cooling test

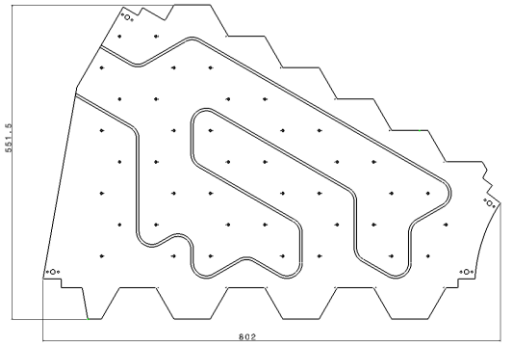
Passive cooling



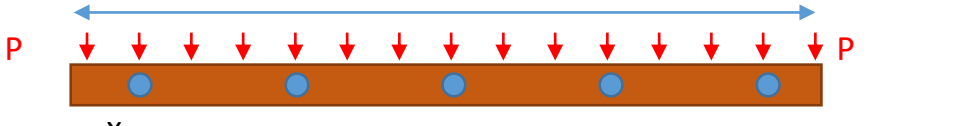
Passive cooling ramp set up test on a 3 layers prototype

- *Passive cooling can lead to more compact solutions depending on the total power to extract and the acceptable temperature gradient*

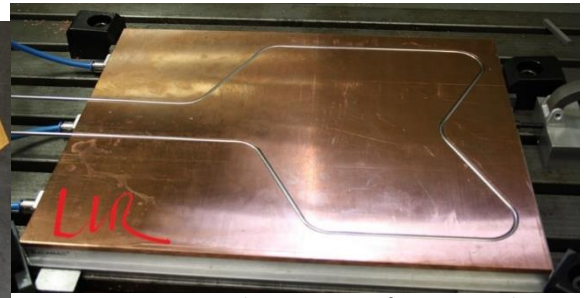
Active cool...g



Copper plate prototype dimensions information



Pipe insertion on a cooling prototype

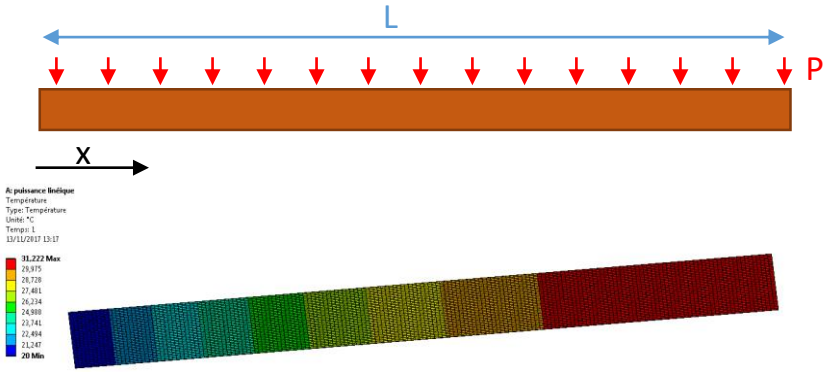


Pipe insertion on a cooling prototype for FEA correlation

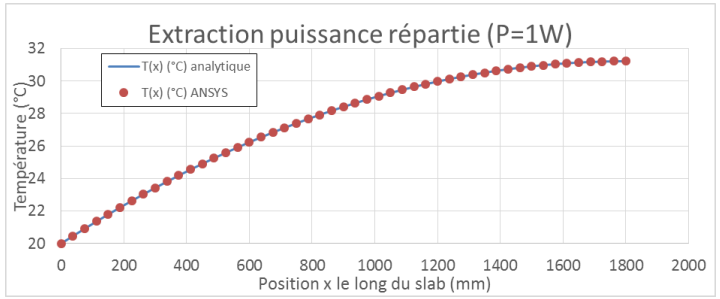
- *Active cooling improves thermal field distribution and can extract much more heat*
- *It requires a qualified pipe insertion process*

Cooling test

Passive cooling

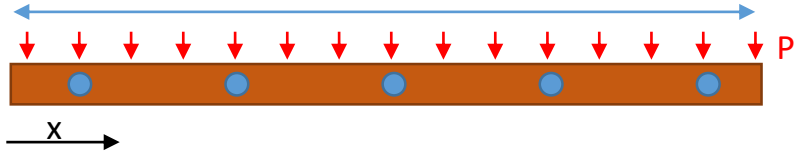


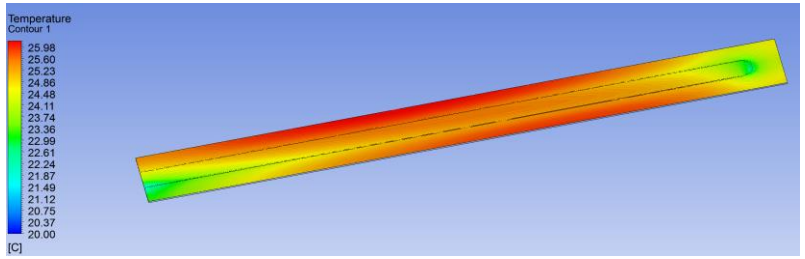
Thermal static FEA analysis thermal field example using ANSYS with 1W extracted



Comparison between thermal static analysis and theoretical approach

Active cooling

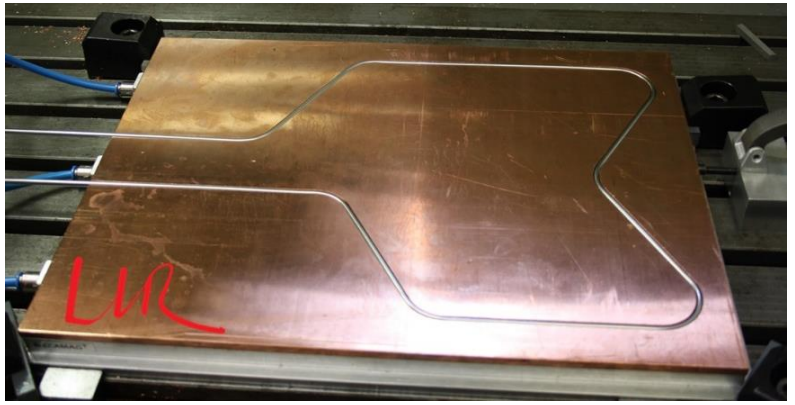


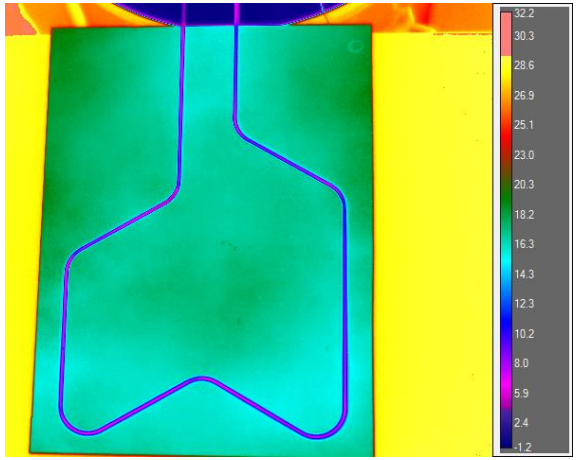


Thermal static CFD analysis thermal field example using Fluent with 100W extracted and water mass flow rate of 7g/s through 1,5mm ID pipe

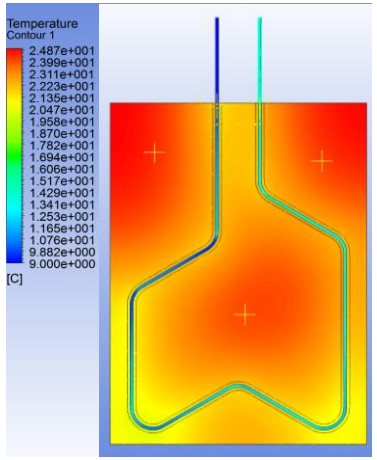
Cooling test

Active cooling pipe insertion test with cold water

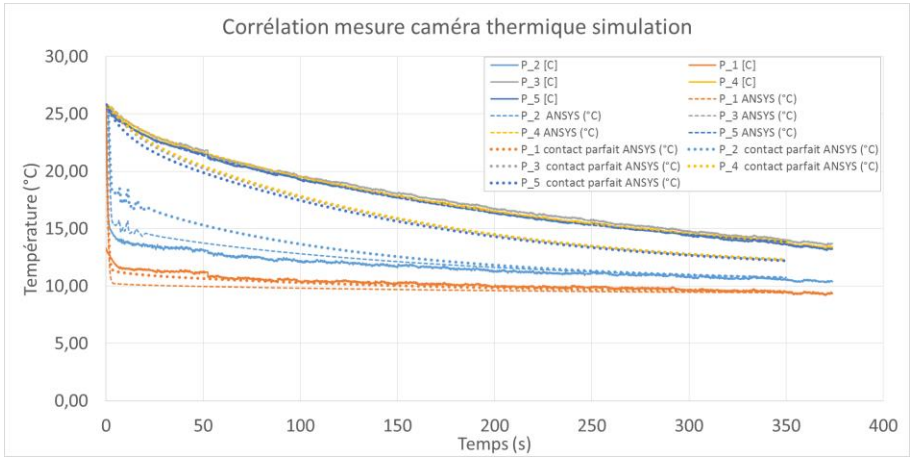




Thermal field registered with an IR camera



CFD correlation results

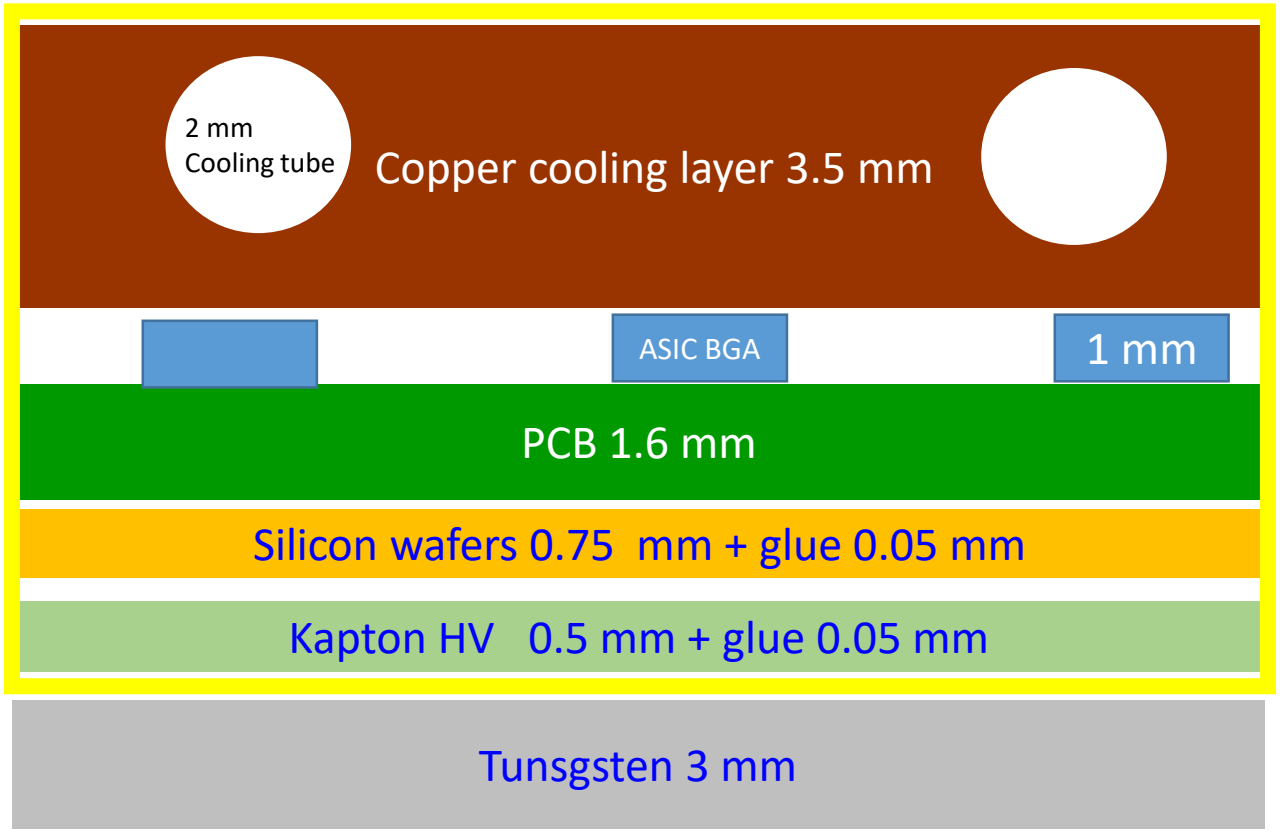


CFD correlation results

- Pipe insertion process introduces some efficiency loss due to the thermal contact resistance.
- The benefit remains significant with regard to a passive cooling

Could it be for FCCee ? YES

REALISTIC (from CMS studies) cross section of the ECAL with active cooling



All thicknesses are based on prototypes… (from ILD or from CMS)

No extrapolation

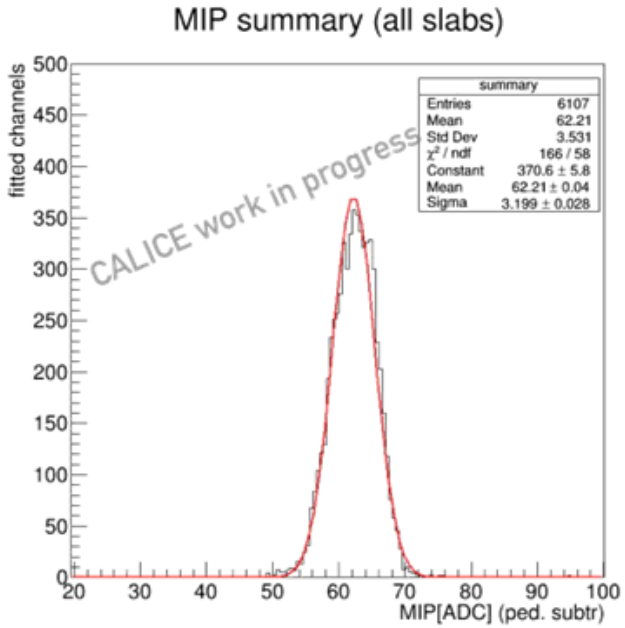
Active cooling for circular machine

On average 9 mm/layer

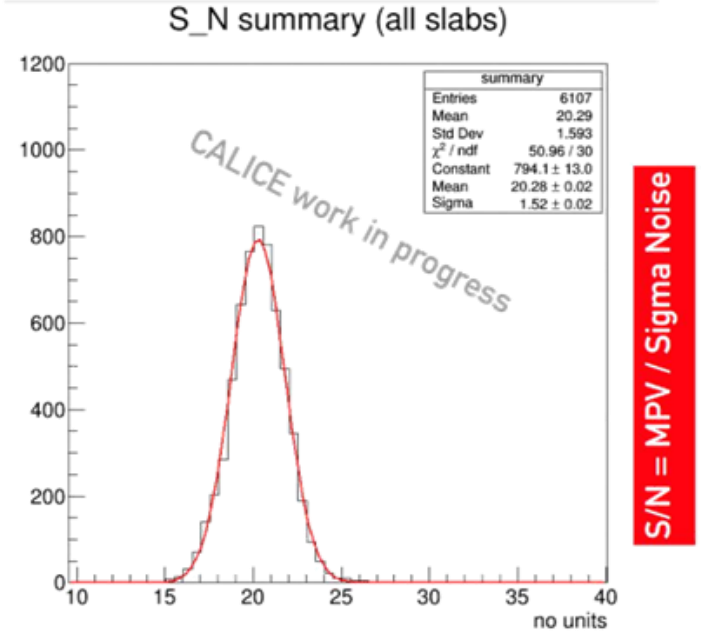
S/N ≈ 20 @mip !!

MIP CALIBRATION RESULTS

- Summary from the MIP fits of the 98% available channels



(MIP position – pedestal position) / pedestal width



S/N = MPV / Sigma Noise

- MPV = 62.2 ADC, sigma= 3.2 ADC (dispersion of 5.1 %)
- S/N = 20.3, sigma = 1.5 (7.4 % dispersion)