# DIAMASIC

F. Rarbi[a], L. Leterrier[b], J. Bouvier[a], S. Drouet[b], L. Gallin-Martel[a], A. Ghimouz[a], O. Rossetto[a], L. Tribouilloy[a], and CAO LPSC

a: LPSC, b: LPC Caen

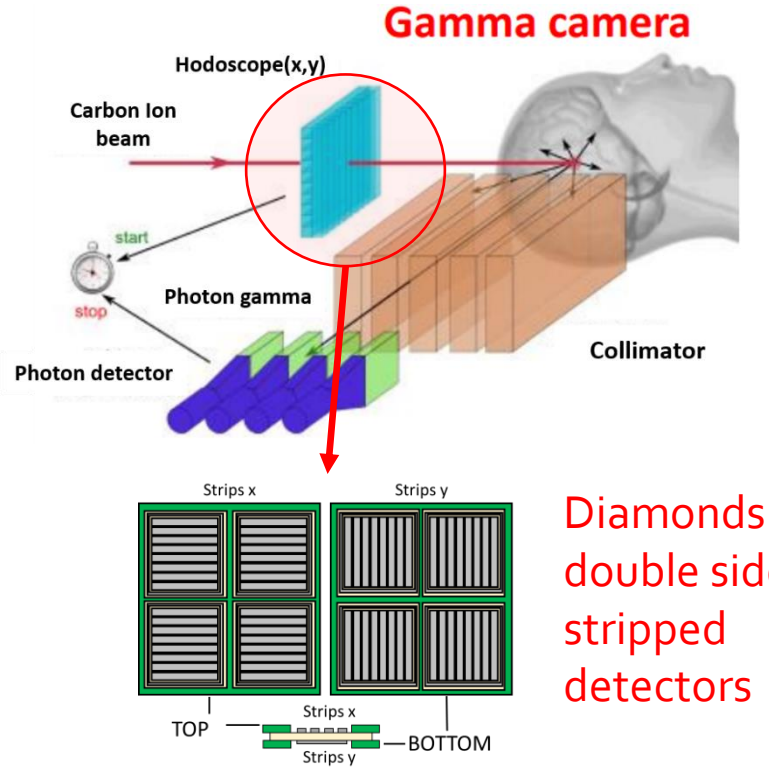
# SCHEDULE

- Project overview
- Technology Readiness Level (TRL)
- Electronic Design
  - Front-end
  - Time to Digital Converter (TDC)
  - Charge to Digital Converter (QDC)
  - Analog to Digital Converter (ADC)
- Conclusions

# PROJECT OVERVIEW

- Medical physics
  - Particle therapy hodoscope: position + time stamp
- Using diamond as detector material:
  - Intrinsic radiation hardness
  - Fast signal risetime enables timing precision of a few tens of ps
  - Low noise
  - Cost
  - Availability of large area
- Beam tagging hodoscope for online ion range verification in hadrontherapy:
  - Time resolution of 100 ps
  - Count rate of 10 MHz/channel
  - Spatial resolution ≈ 1 mm
  - Radiation hard
- Charge measurement
  - ADC with noise shaping principle
  - QDC

| Property | Units | Diamond | Silicon |
|---|---|---|---|
| Band Gap $E_g$ | eV | 5.47 | 1.12 |
| Electron mobility $\mu_e$ | $cm^2$ / V·s | 1700 | 1420 |
| Hole mobility $\mu_h$ | $cm^2$ / V·s | 2100 | 470 |
| Saturation velocity | cm / s | $2\times10^7$ | $1.4\times10^7$ |
| Intrinsic carrier density | $cm^{-3}$ | $<10^3$ | $1.5\times10^{10}$ |
| e/h pair energy | eV | 13 | 3.6 |
| Displacement energy | eV | 37-47 | 15-20 |
| Density | g $cm^{-3}$ | 3.52 | 2.33 |
| Rad length $X_0$ | cm | 12.2 | 9.4 |
| Dielectric constant $\varepsilon_r$ | (relative) | 5.7 | 11.9 |
| Breakdown E-Field | V/µm | 1000 | 30 |
| Resistivity | Ω/cm | $>10^{15}$ | $10^5$ - $10^6$ |




Diamonds double side stripped detectors

More information:
Talk M-L Gallin-Martel

# TECHNOLOGY READINESS LEVEL (TRL)

| Niveau | Définition | Nom synthétique |
|---|---|---|
| TRL1 | Principes de base observés et identifiés | Principe de base |
| TRL2 | Concept technologique et/ou application formulés | Application formulée |
| TRL3 | Preuve du concept analytique et preuve expérimentale de la fonction et/ou de la caractéristique critique | Preuve du concept |
| TRL4 | Vérification fonctionnelle en environnement de laboratoire au niveau composant et/ou maquette | Validation fonctionnelle |
| TRL5 | Vérification en environnement représentatif de la fonction critique au niveau composant et/ou maquette | Modèles à échelle réduite |
| TRL6 | Démonstration en environnement représentatif des fonctions critiques de l'élément au niveau modèle | Validation de la conception |
| TRL7 | Démonstration en environnement opérationnel de la performance de l'élément au niveau modèle | Qualification d'un modèle |
| TRL8 | Système réel développé et jugé apte à l'expérience | Qualification du système réel |
| TRL9 | Système réel ayant été utilisé à l'identique et avec succès lors d'une expérience dans l'environnement idoine. | Opération du système réel |

**TRL initial :**

| TRL1 | **TRL2** | TRL3 | TRL4 | TRL5 | TRL6 | TRL7 | TRL8 | TRL9 |
|---|---|---|---|---|---|---|---|---|

**TRL courant :**

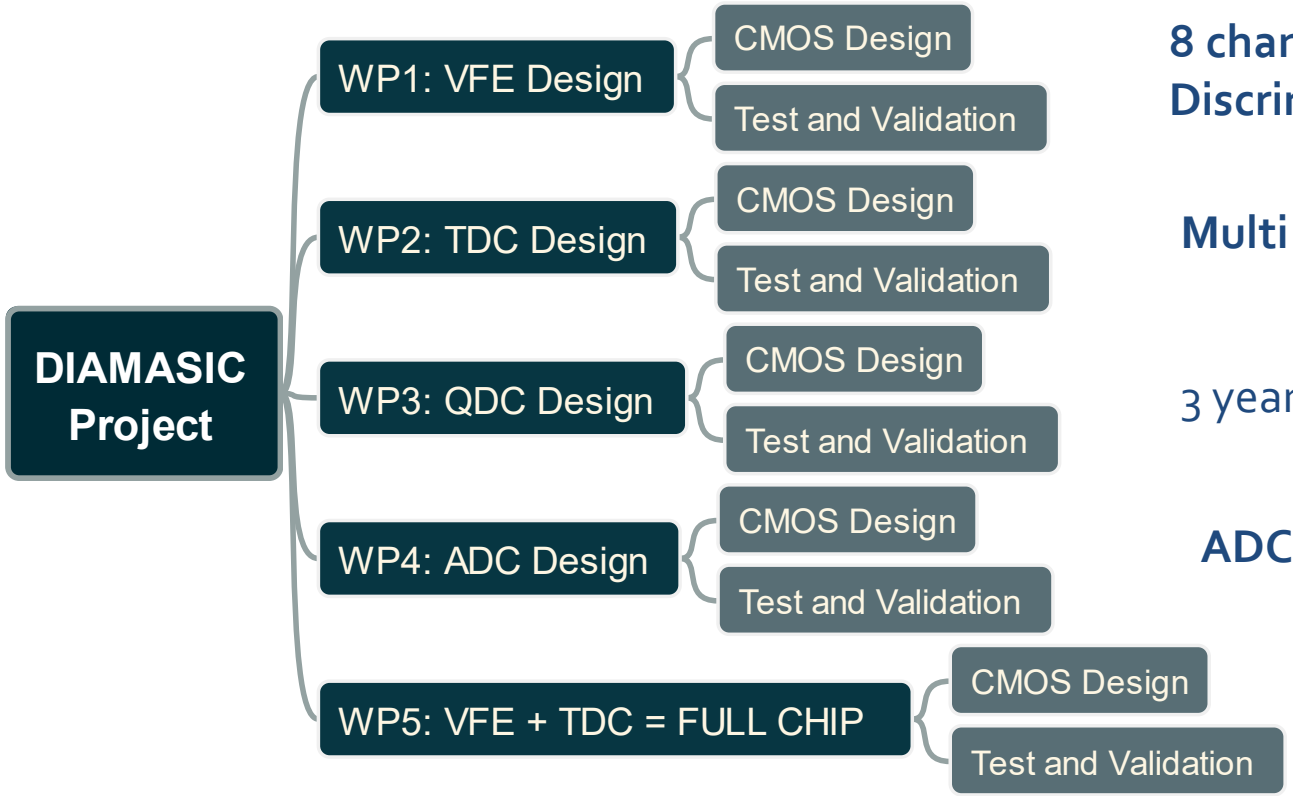
| TRL1 | TRL2 | **TRL3** | TRL4 | TRL5 | TRL6 | TRL7 | TRL8 | TRL9 |
|---|---|---|---|---|---|---|---|---|

**TRL final :**

| TRL1 | TRL2 | TRL3 | **TRL4** | TRL5 | TRL6 | TRL7 | TRL8 | TRL9 |
|---|---|---|---|---|---|---|---|---|

# WP OVERVIEW

Design of multi channel Integrated Circuits:
- CMOS 130nm process technology
- Radiation tolerant technology
- BB130: 1st R&T




**8 channel Trans Impedance Amplifier (TIA) + Fast Discriminator**: PhD EEATS Grenoble

**Multi channel TDC**

3 years apprentice engineer (Grenoble INP – PHELMA)

**ADC with noise shaping**: PhD EEATS Grenoble

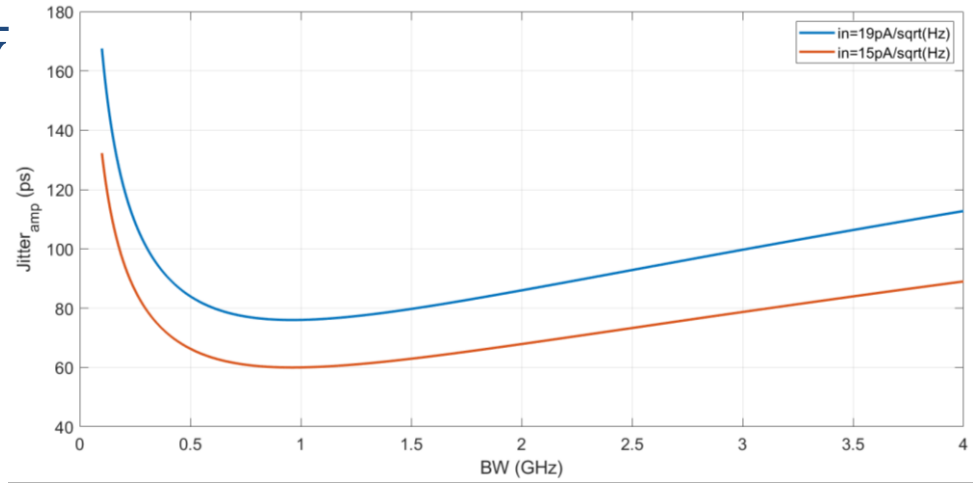
# TIMING RESOLUTION

- Part of PhD work
- Timing resolution defined by: $\sigma_t = \sqrt{\sigma_{Jitter}^2 + \sigma_{TimeWalk}^2 + \sigma_{TDC}^2}$
- For fast system, $\boldsymbol{\sigma_{Jitter}} = \frac{\boldsymbol{T_{rise}}}{\boldsymbol{SNR'}}$

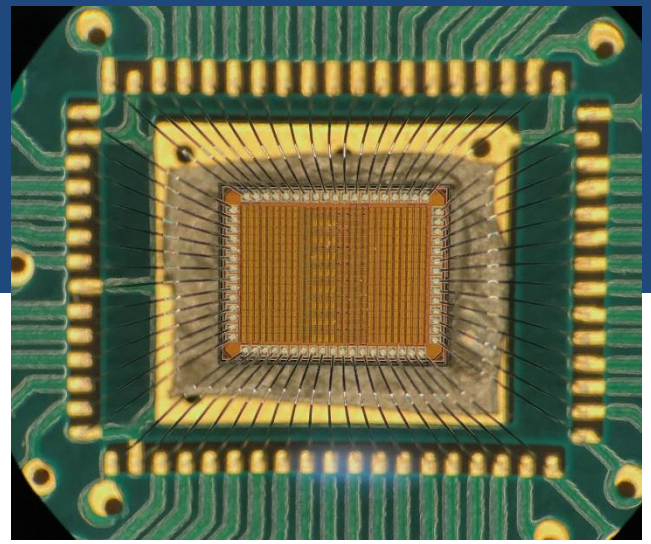
$$SNR = \frac{dV}{\sigma_n} \qquad \sigma_n = G_{TIA} \times i_n \times \sqrt{\alpha \times BW}$$

- We define a new expression:

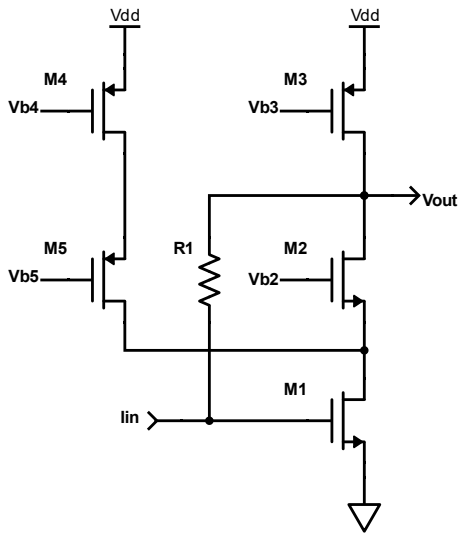
$$\sigma_{Jitter} = \frac{i_n \times \sqrt{\alpha \times BW} \times T_r}{I_{in_{max}}}$$

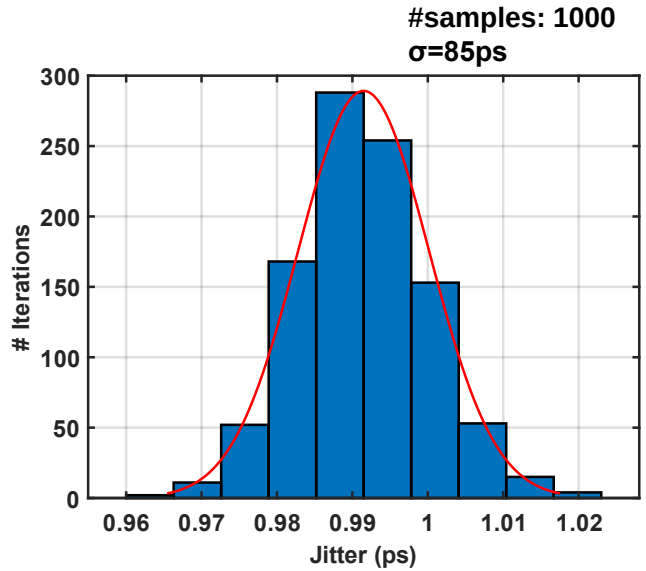


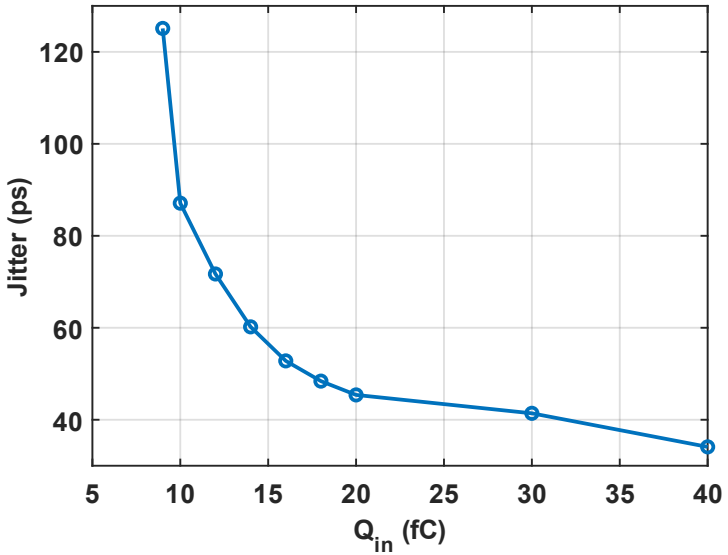
# WP1: VFE DESIGN



- Several FE was studied, designed and tested:
  - Common gate stage
  - LNA stage
  - **Resistive feedback TIA**



# PUBLICATIONS

Abderrahmane Ghimouz et al. “A Preamplifier-discriminator circuit based on a Common Gate Feedforward TIA for fast time measurements using diamond detectors.” In: 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS). 2018, pp. 281–284. DOI: 10.1109/ICECS.2018.8617950

Abderrahmane Ghimouz, et al.. “Systematic high-level design of a fifth order Continuous-Time CRFF Delta Sigma ADC.” In: 2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS). 2021, pp. 1–4. DOI: 10.1109/LASCAS51355.2021.9459156

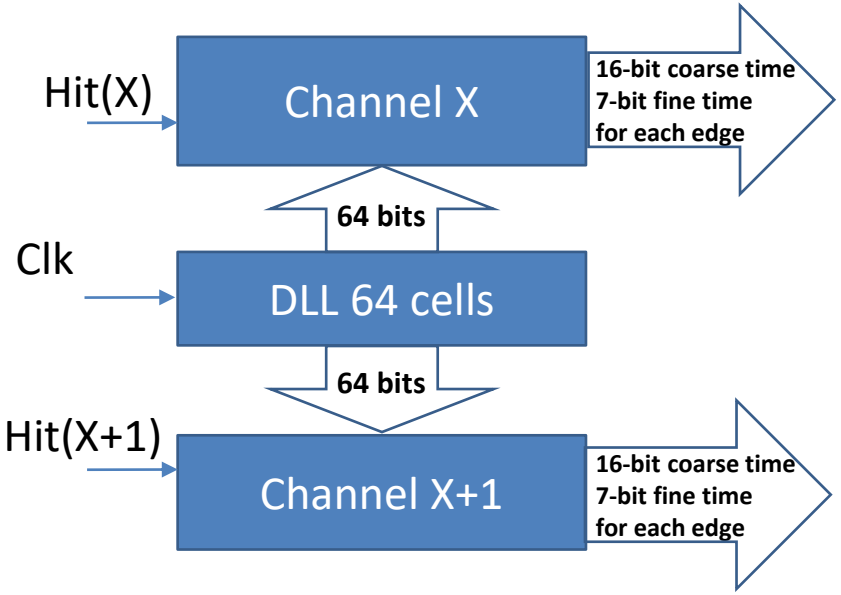
Abderrahmane Ghimouz et al. “A multichannel front-end electronics ASIC for high-accuracy time measurements using diamond detectors.” In: International Conference on Analog VLSI Circuits 2021.(accepted and will be presented soon)

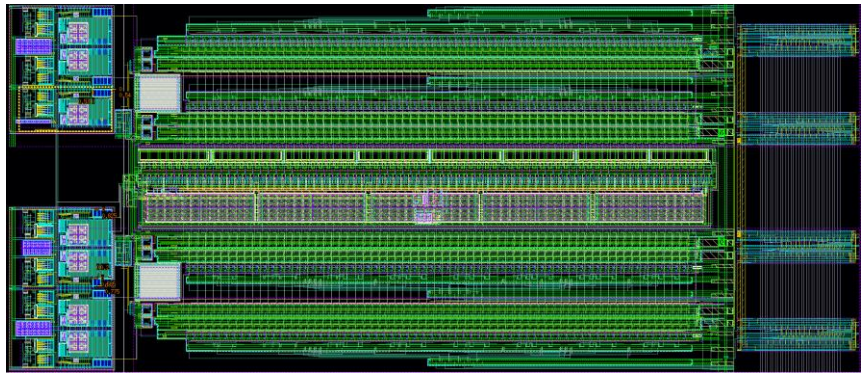
Abderrahmane Ghimouz, et al.. “New Design Approach of Front-End Electronics for high-Accuracy Time Measurement Systems.” In: 2021 28th IEEE International Conference on Electronics, Circuits and Systems (ICECS). 2021 (accepted and will be presented soon)

Abderrahmane Ghimouz, et al.. “DIAMASIC: A multichannel front-end electronics for high-accuracy time measurements for diamond detectors.” In: TWEPP 2021 Topical Workshop on Electronics for Particle Physics. 2021. (Presented and an extended journal paper in under preparation for JINST)

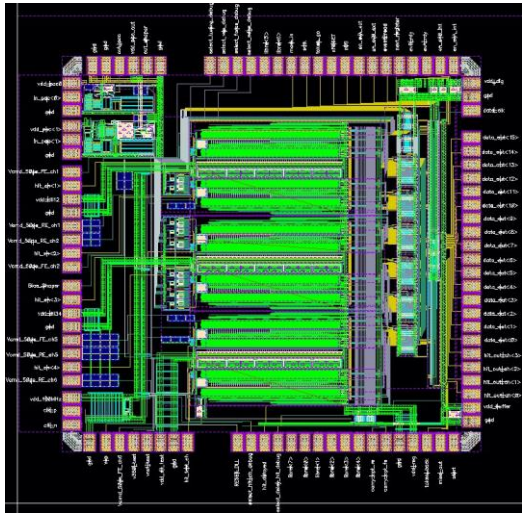
# WP2: TDC DESIGN (1)

- Designed by LPC Caen
- First prototype: 6 channels
- ONE channel composed of 2 TDC sharing the same Delay Locked-Loop (DLL)
  - Can work as ToA or ToT



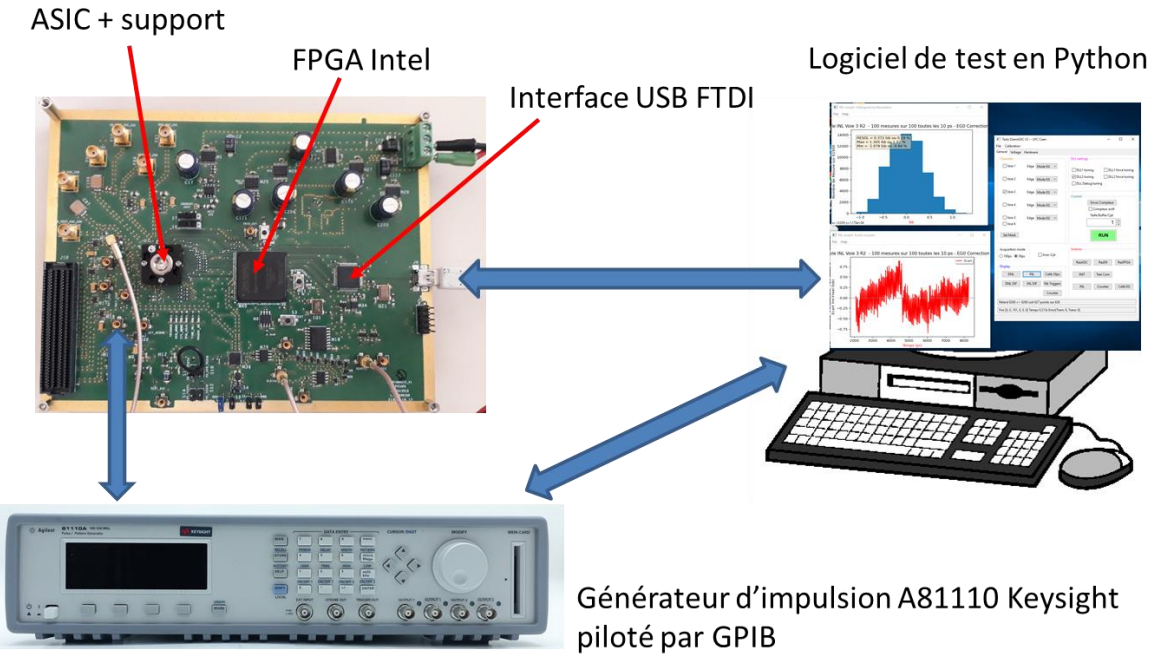



One channel TDC: 557 µm x 1284 µm



DiamASIC_LPCCaen_V2
2.474 mm x 2.340 mm

# WP2: TDC DESIGN (2)



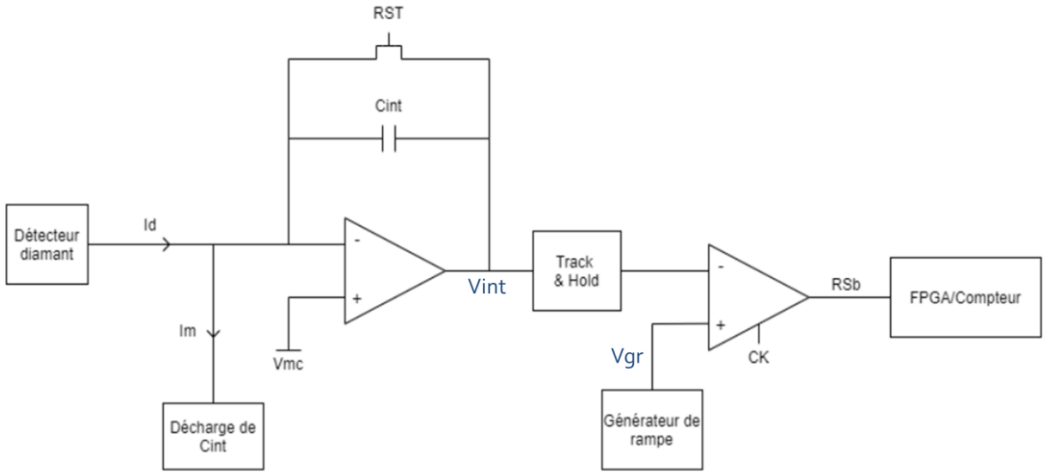

**DNL** measured by code density tests
➔ know the effective size of quantification step

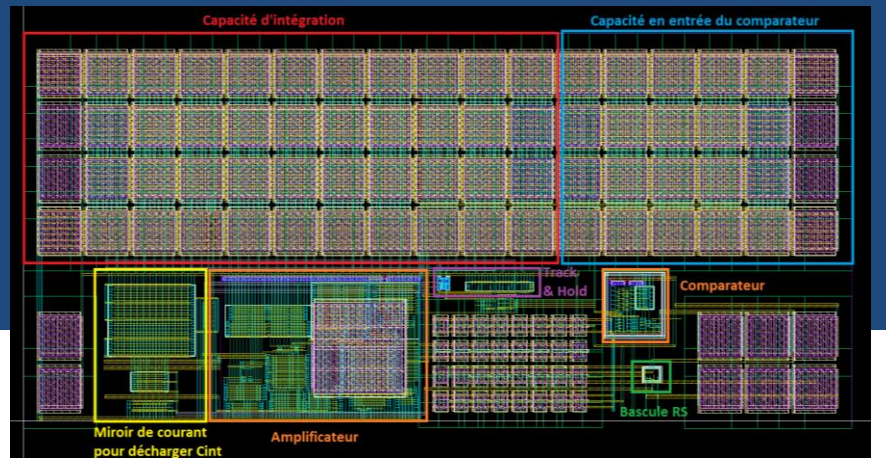
| Parameters | Values | |
|---|---|---|
| **Technology** | CMOS 130nm | |
| **Frequency** | 160MHz | |
| | **Min** | **Max** |
| **DNL** | 16.5 ps | 22 ps |
| **INL** | 46.5 ps | 55 ps |
| **Resolution** | 16.2 ps | 18.2 ps |
| **Power consumption** | 30mW for 6 channels | |

@240MHz ➔ resolution about 12ps

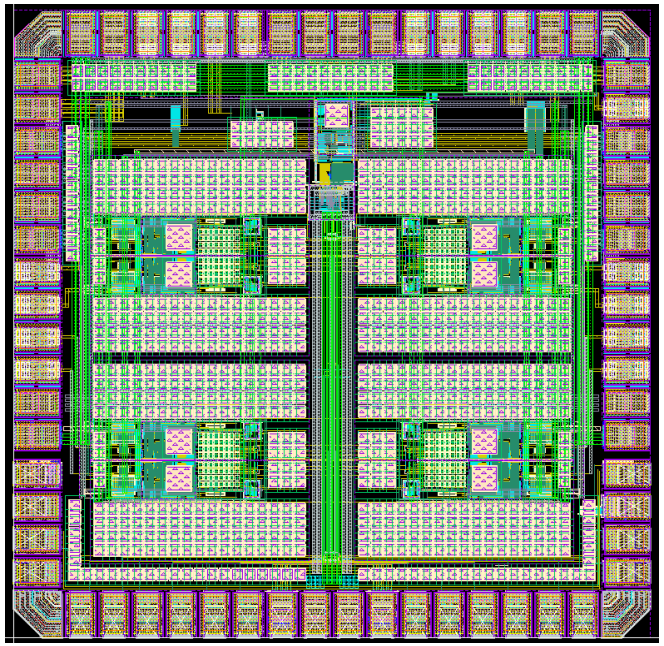
# WP3: QDC DESIGN (1)

- 3 years apprentice engineer (Grenoble INP – PHELMA)
- Specifications:
  - Input Current range: 10nA – 100µA
  - Integration time: 1 ms to 100ms
  - Charge dynamic range of $10^6$



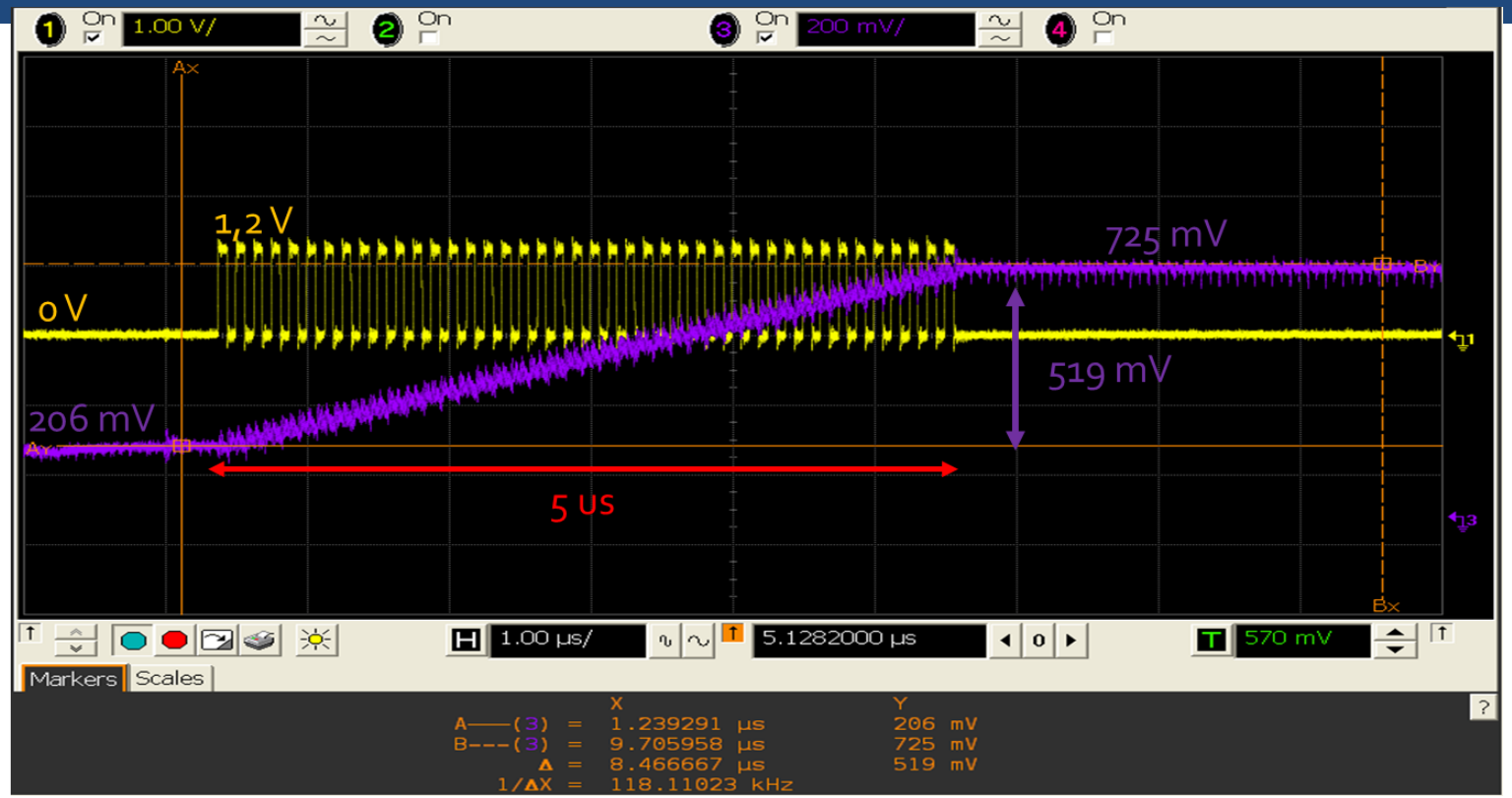




One QDC channel: 523 µm x 247 µm



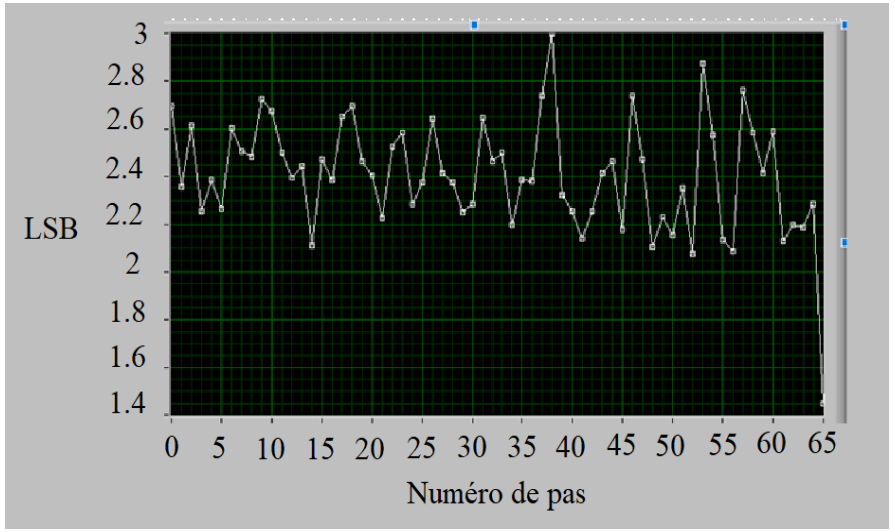
FULL chip:
1.5 mm x 1.5 mm
8 channels
Submitted on May 2021

# WP3: QDC DESIGN (2)



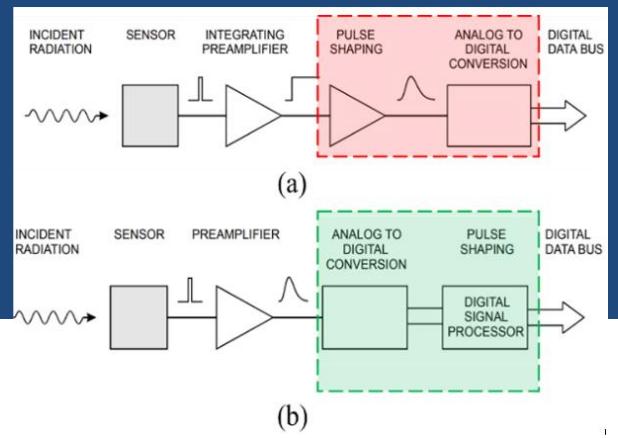

Testing of the ramp generator with 40 steps


**INL: -4 LSB/+2 LSB**



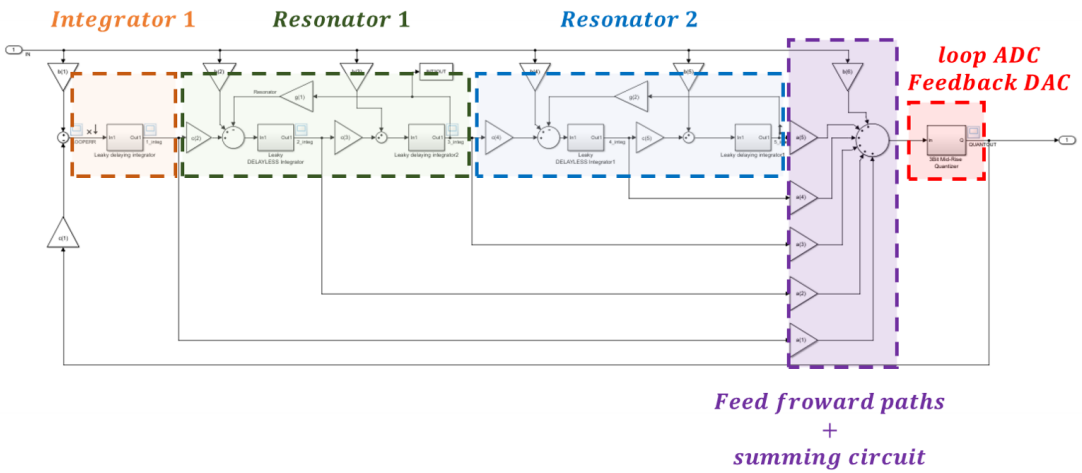

**Max noise: 3 LSB**

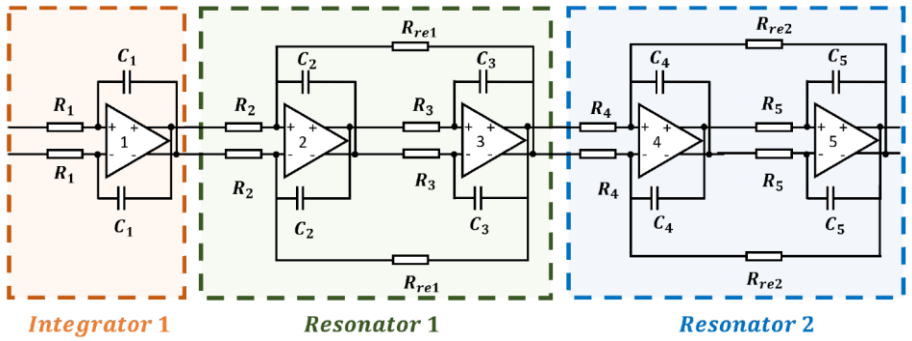
# WP4: ADC DESIGN

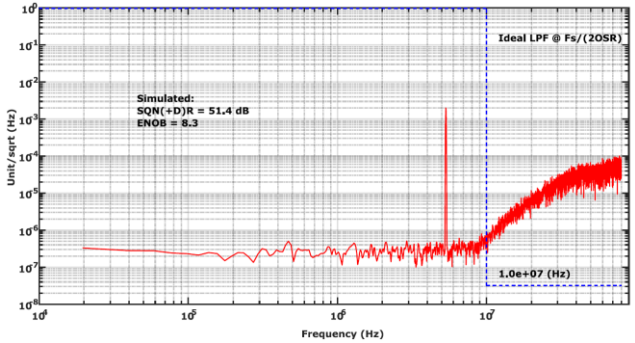



{B. Hallgren, 1991]

- Phd EEATS in microelectronic
  - Started in 2018
  - ***"Design of a continuous time Delta-Sigma modulator for energy measurement using diamond detectors"***
  - Design Top-Down
  - Will be defended on October, 28th 2021 in Grenoble



# PUBLICATIONS

Abderrahmane Ghimouz, et al.. “Systematic high-level design of a fifth order Continuous-Time CRFF Delta Sigma ADC.” In: 2021 IEEE 12th Latin America Symposium on Circuits and System (LASCAS). 2021, pp. 1–4. DOI: 10.1109/LASCAS51355.2021.9459156

Abderrahmane Ghimouz, et al.. “Designing Opamp amplifiers for a 5th order CT CRFF DS ADC using Model-based design paradigm and gm/ID methodology.” In: International Conference on Analog VLSI Circuits 2021. (accepted and will be presented soon).

# CONCLUSION

- IN2P3 R&T project
  - 2 labs: LPSC and LPC Caen
- Design of several IP blocks available through BB130 project
  - Current/Voltage mode DAC, 5 bits
  - SPI control (32 bits)
  - TIA
  - TDC
- PhD student and 3 years apprentice engineer involved in the project