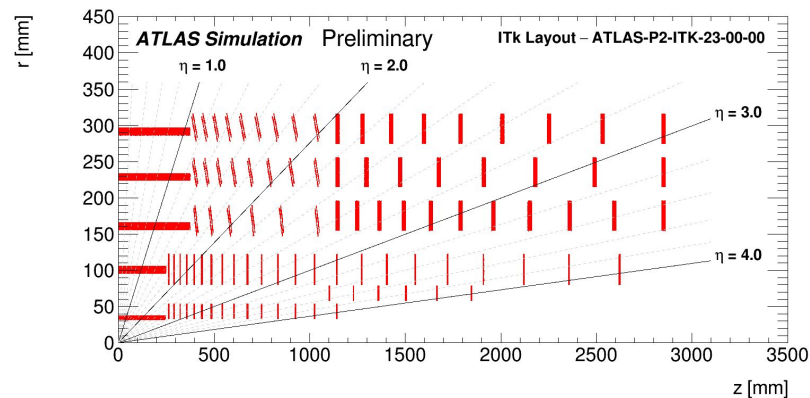
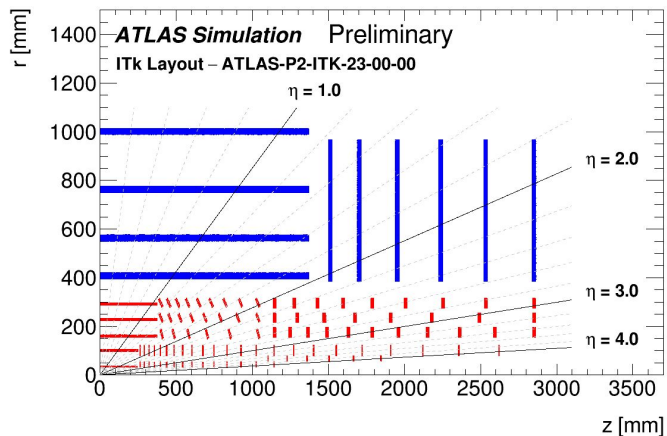


Planar pixel sensors for ATLAS ITk and beyond

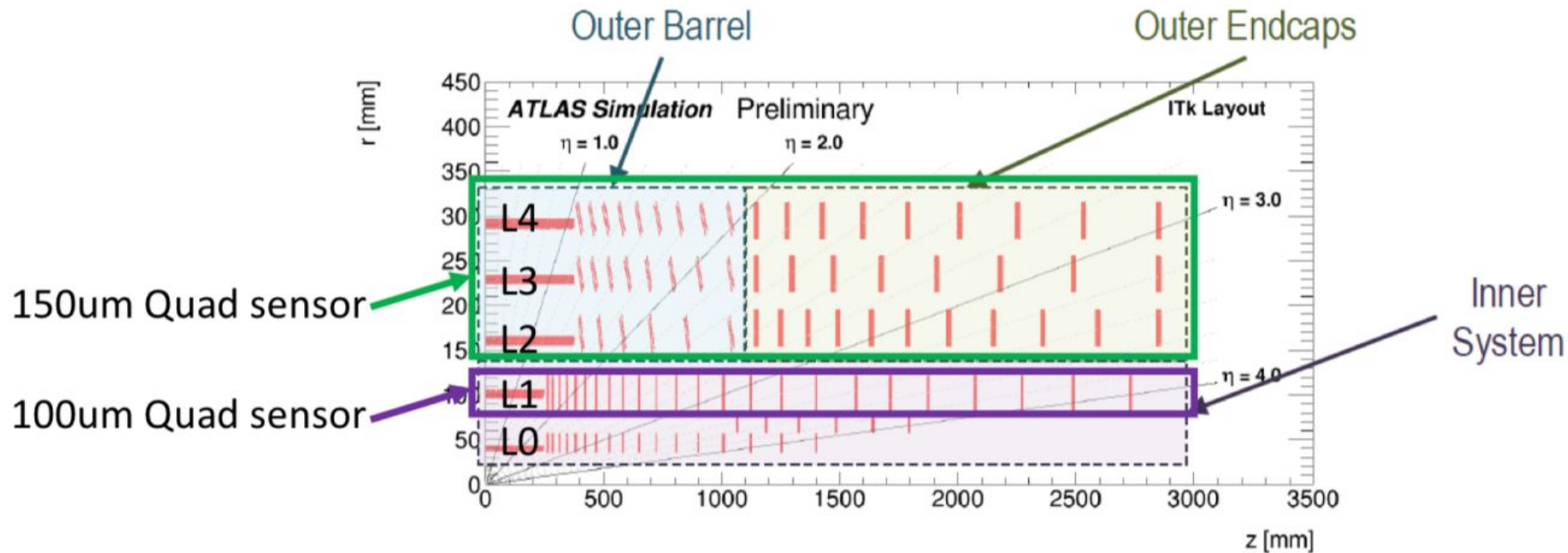
F. Crescioli on behalf of ITk Paris Cluster
(IJCLab, IRFU, LPNHE)

ATLAS & ITk

- ITk is the tracker upgrade for ATLAS @ HL-LHC (Phase-II)
 - Full Silicon tracker: strips & pixels
 - $L_{inst} = 5-7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$
 - Expected Fluence for pixels
 - $1-2 \times 10^{16} \text{ n}_{eq}/\text{cm}^2$ for innermost layer (3D pixel)
 - $2-3 \times 10^{15} \text{ n}_{eq}/\text{cm}^2$ for outer layers (planar pixel)

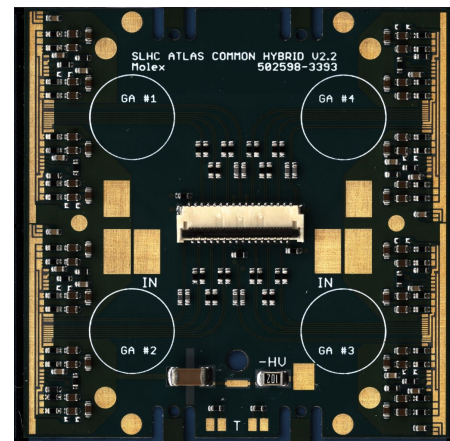
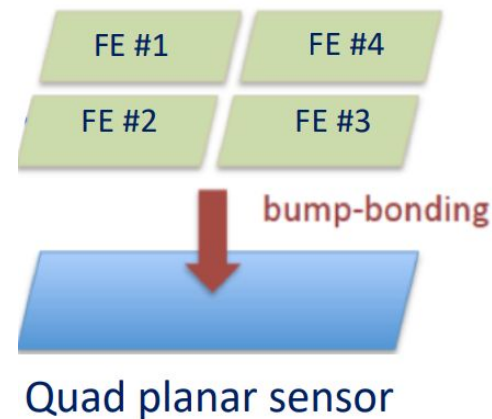


ITk pixel layout



ITk planar sensor pixels

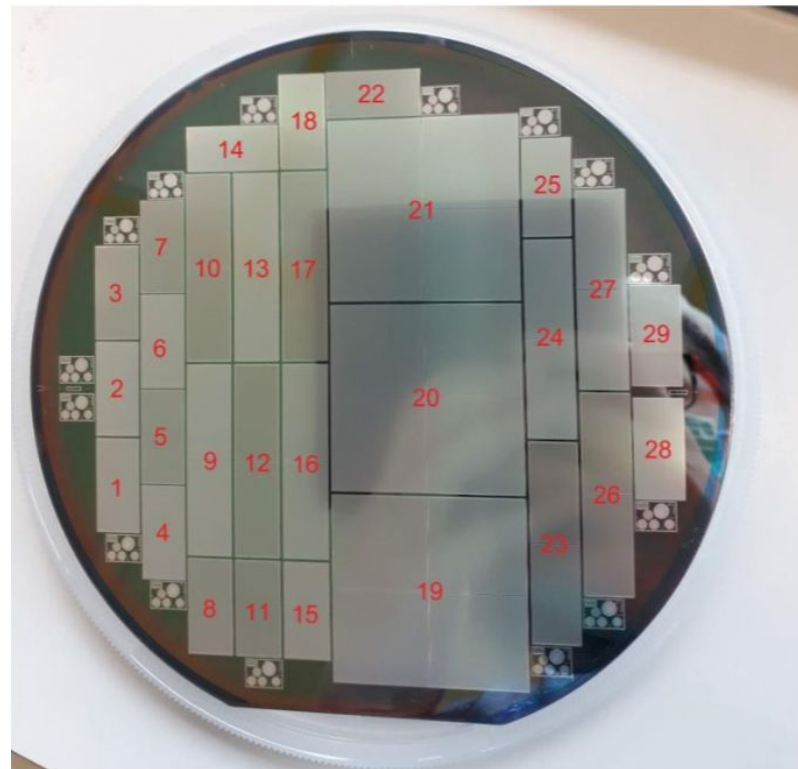
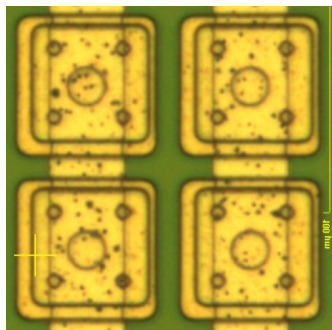
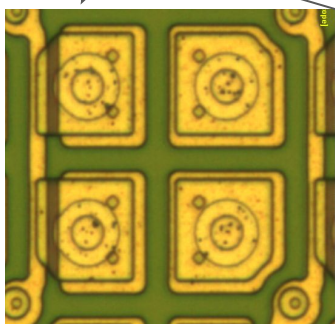
- Pitch $50 \times 50 \mu\text{m}^2$
- n-in-p technology
- 100 μm thin sensors for L1
- 150 μm thin sensors for L2-L4
- ITk pixel FR chip is $20 \times 19.2 \text{ mm}^2$ (400x384)
 - Planar sensors produced for 4x FE chips: Quad module



R&D sensors for ITk

- Production 2019 @ FBK
- Single (RD53A), double (RD53A) and quad (ITk) design
- 50-**100-150** um thickness
- Biasing scheme

- Punch through (different designs)
- Temporary metal



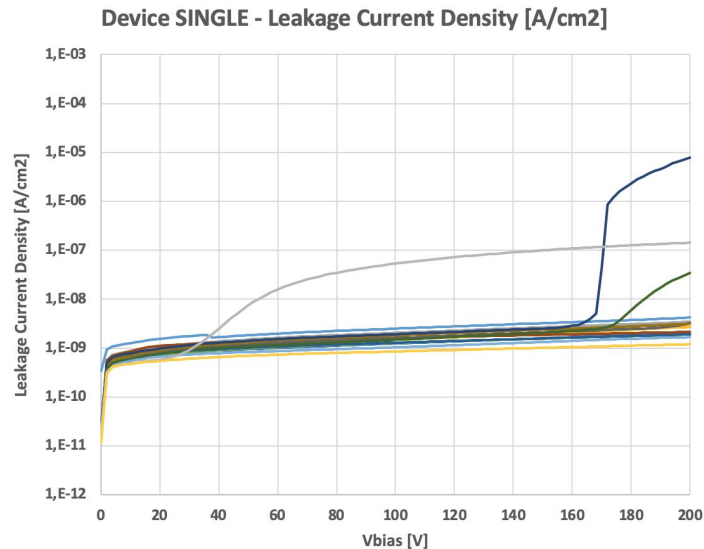
R&D sensors for ITk

Depletion voltage:

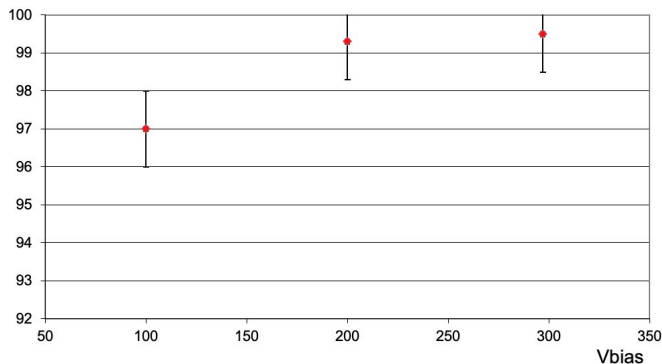
- 10-15 for 100 μm
- 20-30 for 150 μm

Tested at DESY after irradiation

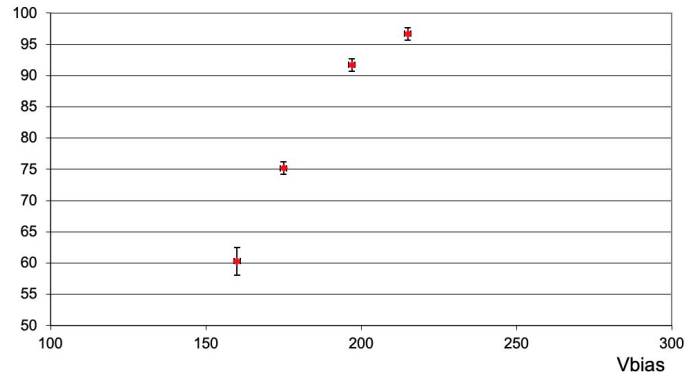
- $2 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$
- $5 \times 10^{15} \text{ n}_{\text{eq}}/\text{cm}^2$



Efficiency at fluence $2 \times 10^{15} \text{ neq}$



Efficiency at fluence $5 \times 10^{15} \text{ neq}$

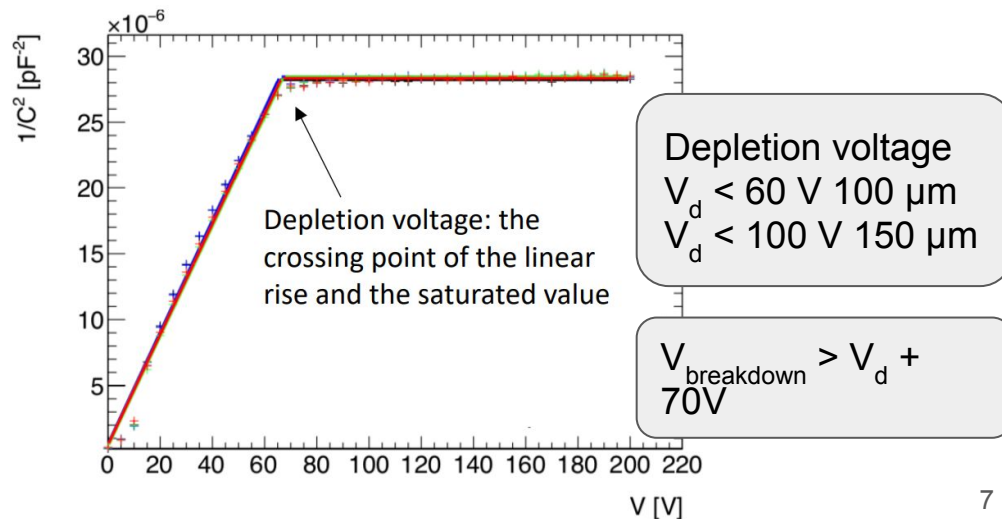


Most devices
have breakdown
> 200V

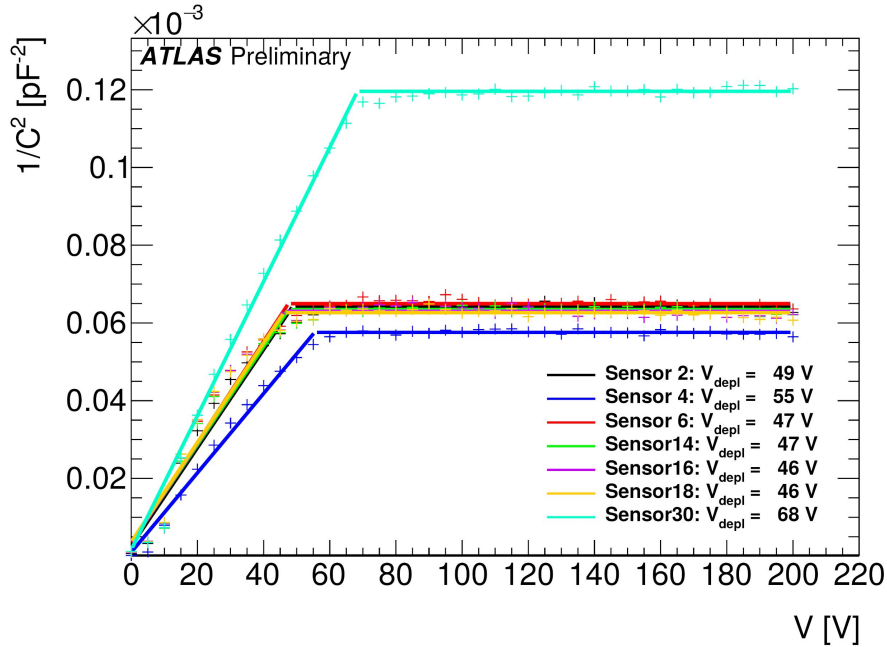
Market Survey for ITk

- Several vendors applied to supply ATLAS of ITk sensors
- In order to qualify fairly each vendor a strict procedure has been established:
Market Survey
- ITk institutes participate by performing the required measurements
 - Metrology
 - Electrical measurements

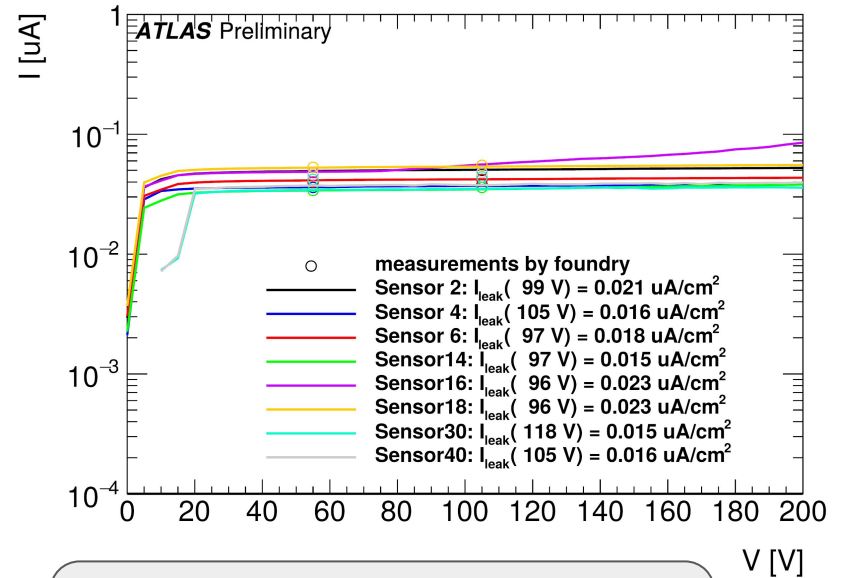
Deviation of average wafer thickness variation with respect to the specified thickness	$\leq 15 \mu\text{m}$
Physical sensor thickness variation inside a single sensor	$\leq 15 \mu\text{m}$
Wafer bow of 6" size	$\leq 100 \mu\text{m}$
Wafer bow of 8" size	$\leq 150 \mu\text{m}$
Sensor bow (4-chip geometry)	$\leq 25 \mu\text{m}$



ITk Market Survey Electrical Measurements



MS public plots



Results include measurements done within the Paris ITk Cluster of labs

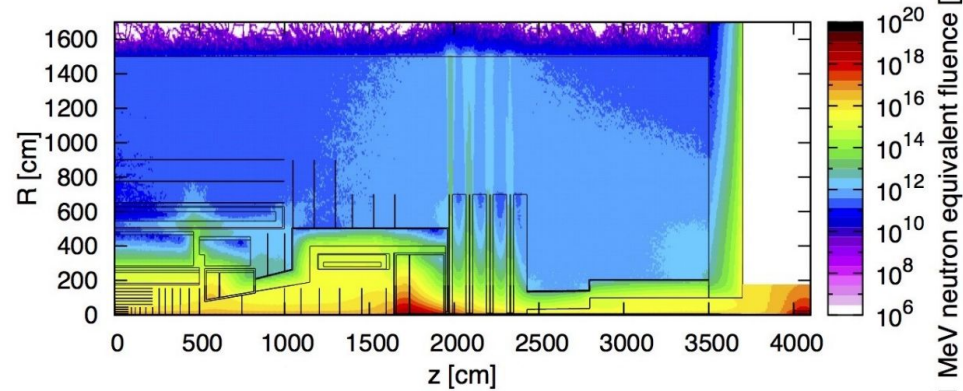
Beyond ITk

- Future **hadron** colliders will have much higher fluence
- FCC-hh up to $5.5 \times 10^{17} n_{\text{eq}}/\text{cm}^2$
- Thin sensors to keep the material budget very low

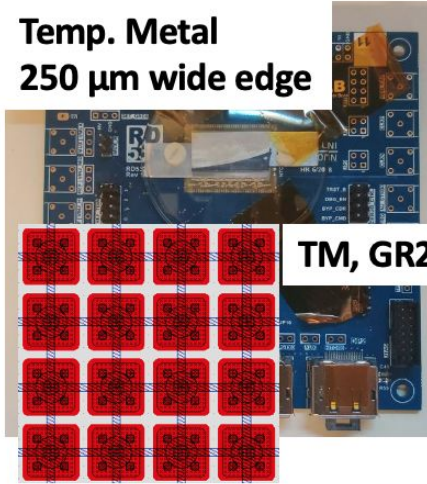
Long-term damage for Tracker after 30ab^{-1}

R [mm]	z[m]	Dose [MGy]	1 MeV equivalent Fluence [cm^{-2}]
25	0	320	$5.5 \cdot 10^{17}$
60	0	88	$1.25 \cdot 10^{17}$
100	0	40	$6 \cdot 10^{16}$
150	0	23	$3.3 \cdot 10^{16}$
270	0	8.8	$1.51 \cdot 10^{16}$
900	0	0.65	$3.2 \cdot 10^{15}$
25	5	410	$3.7 \cdot 10^{17}$
50	16	250	$2 \cdot 10^{17}$

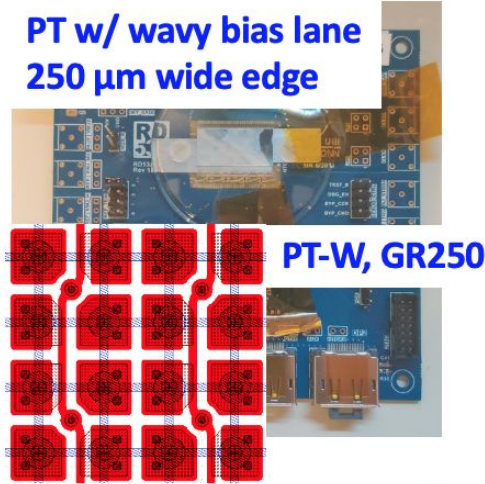
Courtesy of M.I.Besana



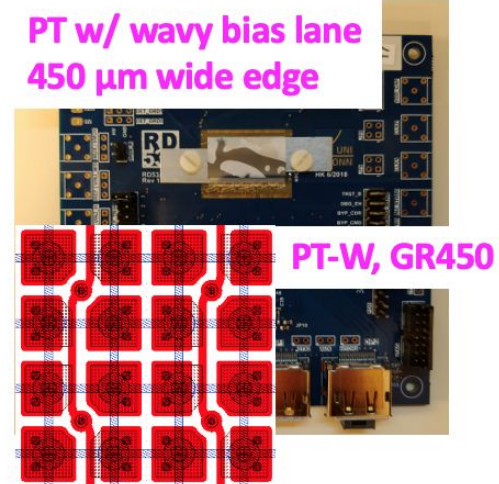
Temp. Metal
250 μm wide edge



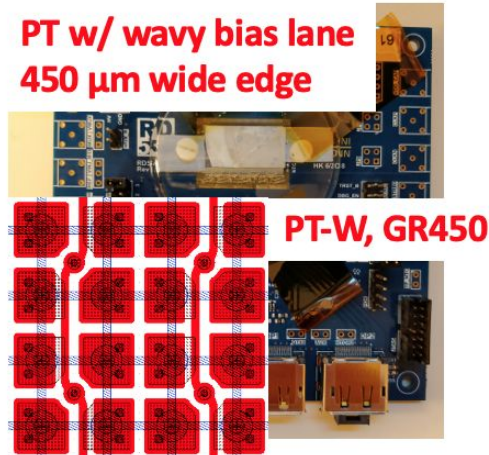
PT w/ wavy bias lane
250 μm wide edge



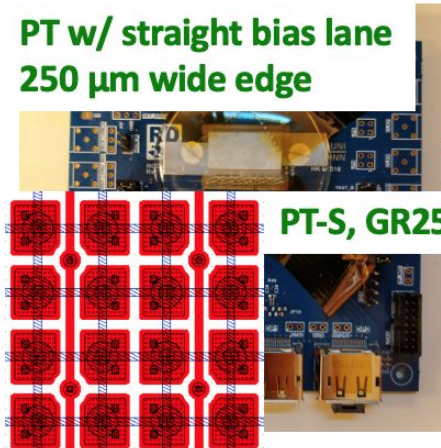
PT w/ wavy bias lane
450 μm wide edge



PT w/ wavy bias lane
450 μm wide edge



PT w/ straight bias lane
250 μm wide edge



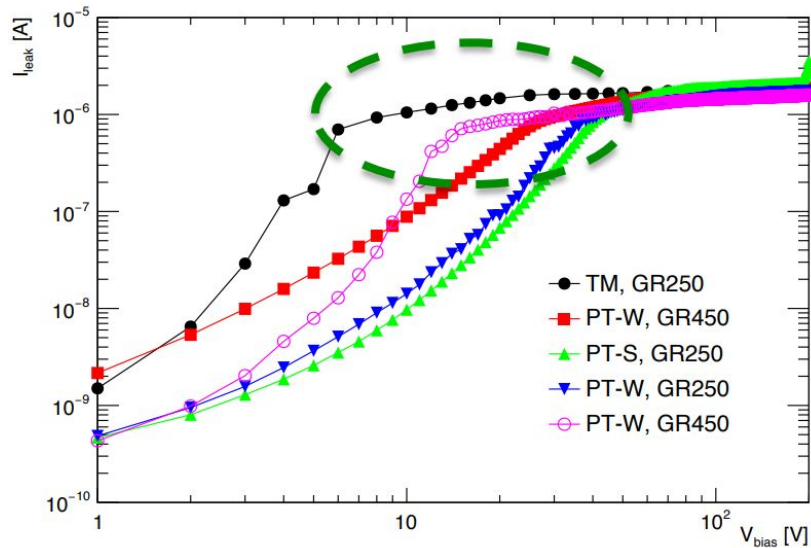
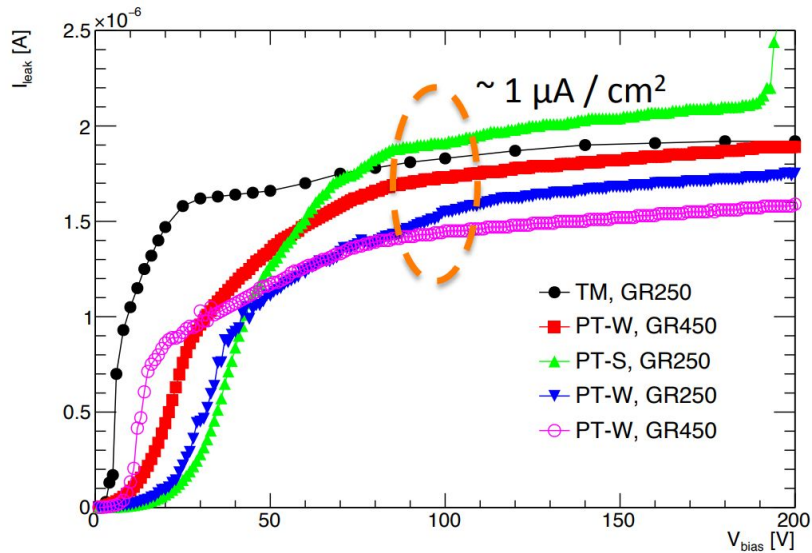
Unfortunately roc
unresponsive so no
data for this design

50 μm thickness
production 2019

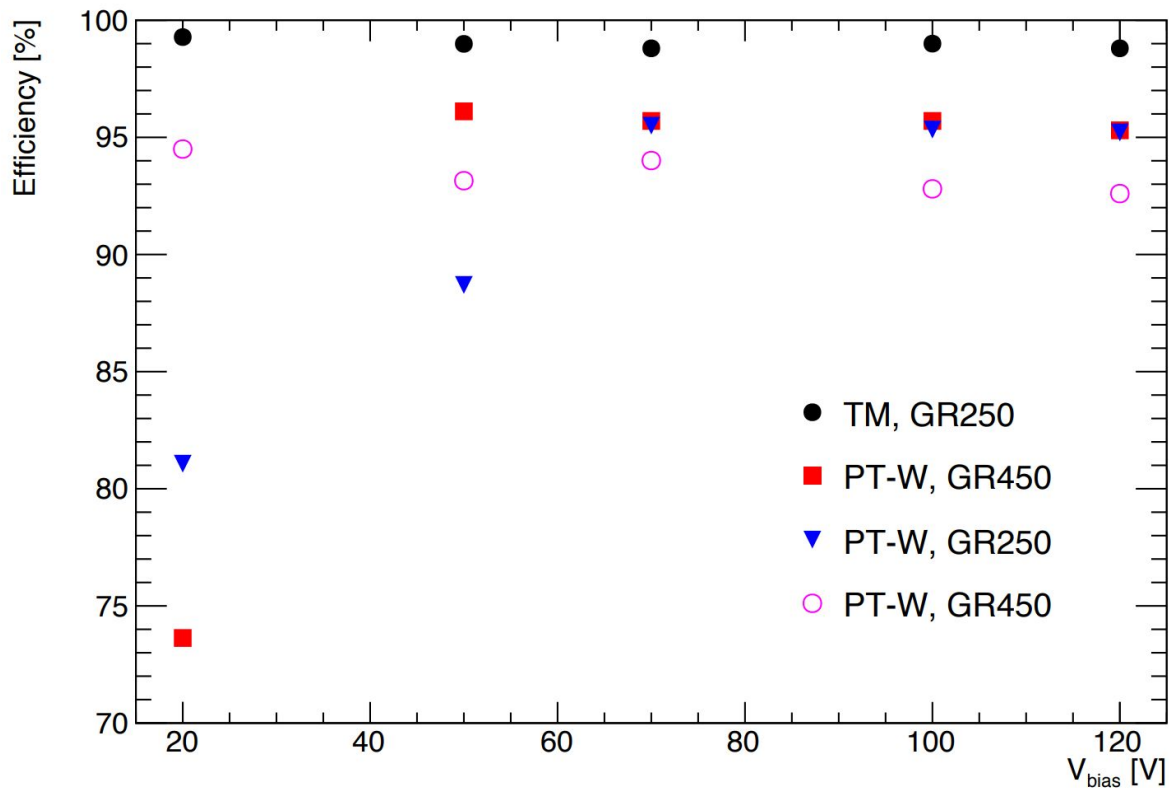
50 um thickness: IV Curve

Breakdown > 200 V

Depletion 10-30 V

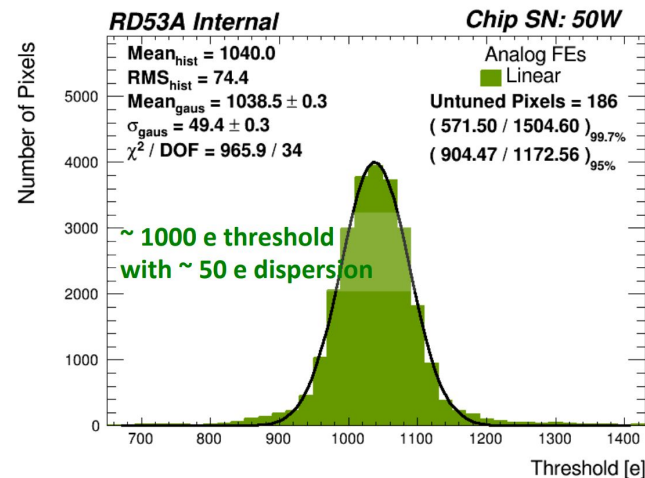


50 um thickness: hit efficiency



Efficiency 99% for temporary metal design

94-96% for punch through design (see next slide)

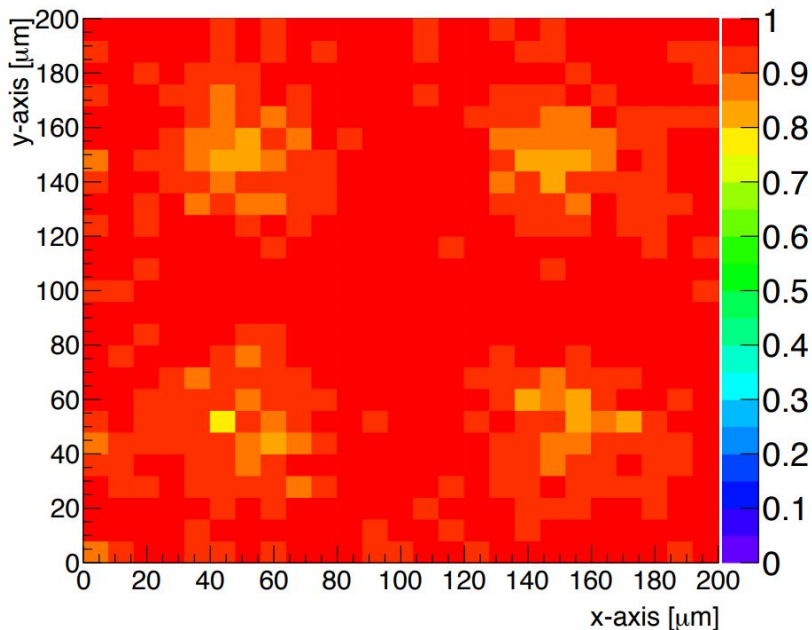


50 μm thickness

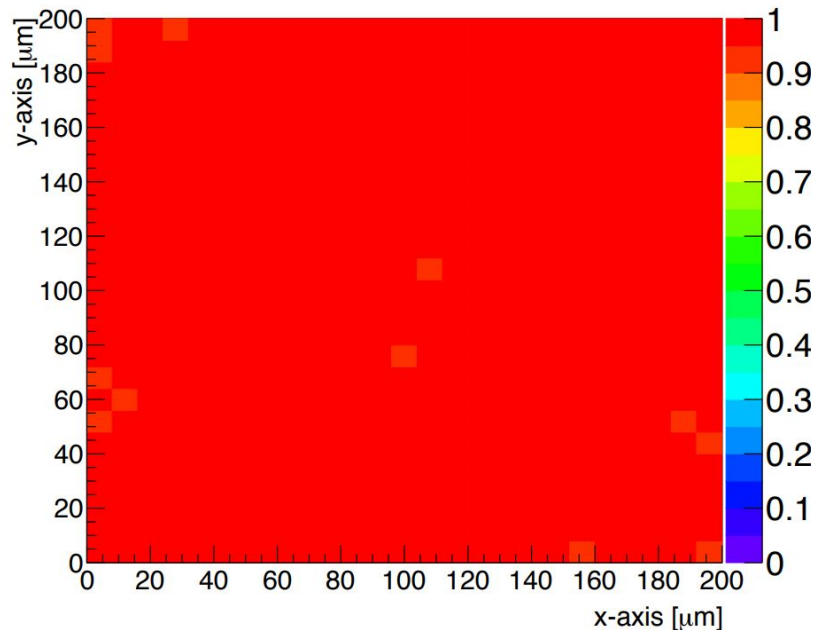
Localized loss of efficiency due to the punch through structure

N.B. tracks at normal incidence

Hit-eff. folded in a 4x4 pixel map



PT-W, GR250



TM, GR250

Conclusions

- The ITk upgrade for the ATLAS silicon tracker for HL-LHC is preparing for the production phase
 - Planar pixel sensors will be used in all but the innermost pixel layer
 - 100 μm and 150 μm sensors from various vendors are going through a qualification stage called Market Survey
 - All ITk institutes including the Paris Cluster institutes are involved in the Market Survey effort through metrology and electrical measurements
- Future hadronic colliders impose light and high efficient silicon sensors for tracking in unprecedented harsh environments
 - Thin n-on-p pixels are promising candidates
 - Small pitches are becoming available
 - Very thin sensors (50 μm) show promising results before irradiation
 - two of them will be tested in DESY in next available test beam after irradiation to 5×10^{15} $n_{\text{eq}}/\text{cm}^2$